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Analysis, Design and Implementation of a High Efficiency Multilevel Converter for Renewable Energy Systems

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Abstract

Stand-alone renewable energy systems are used to supply electricity to remote areas where access to the utility grid is not available. Mostly common systems store energy in battery banks in order to compensate intermittence and peak power limitation of renewable energy sources. Because common appliances are designed to operate with the utility, a device capable to convert the DC voltage of batteries into standard AC voltage is necessary. This device is called inverter, and this work presents the analysis, design and implementation of an inverter based on a multilevel topology.

Multilevel inverters are mainly used in high power applications, where they have proved to be reliable and robust. They operate with low frequency and present high efficiency. Current demand on reliable, efficient and robust inverters for renewable energy systems has extended multilevel inverters application to small power systems as well. This work shows that only few multilevel topologies are suitable to implement battery inverters, such as the one here adopted, and relevant contributions to the analysis and simulation of high-resolution multilevel inverters are presented.

The adopted topology is based on a line-frequency transformer with several isolated outputs that are combined through static power switches in order to produce a multilevel voltage waveform. This topology is suitable to implement high-resolution multilevel inverters and it is capable to operate with bi-directional power flow.

A 63-level inverter of 3 kVA was implemented and successfully tested with both experimental and standard appliances, presenting peak efficiency of 96.0 % and no-load consumption of 18.6 W. A new method to identify and correct unbalanced load condition was specially developed for the proposed inverter.

In comparison with equivalent commercial inverters, the proposed inverter presented the best overall efficiency for any load demand higher than 270 kWh/month. Finally, through further improvements in the multiple-winding transformer and use of better switches, it is expected that the proposed inverter can present the best feasible overall efficiency for any realistic load profile in stand-alone energy systems.

Keywords: renewable energy, multilevel inverter, high efficiency.

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Zusammenfassung

Netzautarke erneuerbare Energiesysteme verwendet man, um entlegene Gebiete, die keinen Zugang zum Energieversorgungsnetz haben, mit Elektrizität zu versorgen. Die meisten Systeme speichern die erzeugte Energie in Akkumulatoren, um Stromabschaltungen zu vermeiden und Lastspitzen zu kompensieren. Da die meisten Haushaltgeräte und elektrischen Verbraucher auf das Wechselstromnetz ausgelegt sind, ist es nötig, den Gleichstrom, den die Batterien liefern, in Wechselstrom zu konvertieren. Für diese Konvertierung wird ein Apparat verwendet, den man Wechselrichter nennt. Die Analyse, der Aufbau und die Implementierung von einem Wechselrichter, basierend auf einer besonderen Mehrpunkt-Topologie, sind in dieser Arbeit präsentiert.

Mehrpunkt-Wechselrichter werden hauptsächlich in Hochleistungsanwendungen verwendet, wo sie sich als zuverlässig und robust erwiesen haben. Sie arbeiten mit niedriger Frequenz und haben einen hohen Wirkungsgrad. Aktuelle Nachfrage nach zuverlässigen und robusten Wechselrichtern für erneuerbare Energiesysteme hat Mehrpunkt-Wechselrichter für Kleinleistungsanwendungen hervorgebracht. Diese Arbeit zeigt, dass nur wenige Mehrpunkt-Topologien geeignet sind, um als Batterie-Wechselrichter zu funktionieren, so wie die hier gewählte Topologie. Diese Arbeit enthält darüber hinaus auch relevante Beiträge zur Analyse und Simulationen von Hochauflösenden Mehrpunkt-Wechselrichtern.

Die hier präsentierte Topologie basiert auf einem Netzfrequenz-Transformator mit mehreren isolierten Ausgangsspannungen, die mit statischen Leistungsschaltern kombiniert wurden, um eine Mehrpunkt-Spannungskurvenform zu erzeugen. Mit dieser Topologie können Hochauflösende Mehrpunkt-Wechselrichter mit bidirektionalem Leistungsfluss realisiert werden.

Ein 63-Punkt Wechselrichter von 3 kVA wurde gebaut und sowohl unter Laborbedingungen als auch mit üblichen Haushaltgeräten erfolgreich getestet. Er erreichte eine maximale Effizienz von 96,0% und zeigte einen Leerlaufverbrauch von 18,6 W. Eine neue Methode zur Identifizierung und Korrektur unausgeglichener Lastzustände wurde speziell für den vorgeschlagenen Wechselrichter entwickelt.

Im Vergleich zu kommerziellen Modellen erreichte der vorgeschlagene Wechselrichter die beste Gesamteffizienz für einen Verbrauch über 270 kWh/Monat. Durch weitere Verbesserungen am mehrfach gewickelten Transformator und durch Verwendung besserer Schalter wird der vorgeschlagene Wechselrichter den besten Wirkungsgrad für alle realistischen Lastprofile in netzautarken erneuerbaren Energiesystemen haben.

Stichwörter: Erneuerbare Energie, Mehrpunkt-Wechselrichter, hohe Effizienz.

Gratias tibi agimus, Pater noster, pro universis beneficis tuis.

In memoriam of my father Elias

★20th August 1936, †29th November 2004

To my Family

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Nomenclature

Symbol/Acronym	Unit	Description
η	[%]	Inverter efficiency
η_c	[%]	Conversion efficiency (extended model)
η_{cw}	[%]	Weighted conversion efficiency (extended model)
η_{pk}	[%]	Peak efficiency
θ_n	[^{o}]	n^{th} switching angle
C_n	[F]	Designator of the snubber capacitors of the n^{th} output cell
$C_{n/x}$	[F]	Designator of one snubber capacitor (n^{th} cell, x = a,b)
dv/dt	[V/s]	Voltage change rate
E	[V]	Voltage of a generic DC source
E_C	[kWh]	Monthly energy consumption
E_L	[kWh]	Monthly energy loss
f_n	[Hz]	Switching frequency of the n^{th} cell
f_L	[Hz]	Line frequency
I_1	[A]	Current at transformer primary (transformer model)
I_2	[A]	Current at transformer secondary (transformer model)
I_d	[A]	Rated continuous drain current of a MOSFET
I_m	[A]	Magnetizing current
I_{m1}	[A]	Magnetizing current peak (positive semi-cycle)
I_{m2}	[A]	Magnetizing current peak (negative semi-cycle)
I_n	[A]	RMS current through the n^{th} output-stage switch
I_{os}	[A]	Output-stage RMS current
$I_{os}(t)$	[A]	Instantaneous output-stage current
I_{ospk}	[A]	Peak value of the output-stage current
I_p	[A]	Transformer primary RMS current
$I_p(t)$	[A]	Instantaneous transformer primary current

I_x	[A]	Identifier for a particular current (figures 4.26 and 4.31)
kW_p	[kW]	Peak power expressed in kW
L_1	[H]	Leakage inductance of the transformer primary
L_2	[H]	Leakage inductance of the transformer secondary
L_m	[H]	Magnetizing inductance of a transformer
$L_p(P_o)$	[%]	Load profile
M_i	[-]	Modulation index
MWp	[MW]	Peak power expressed in MW
N	[-]	Number of cells
p	[-]	Number of steps in a quarter-cycle of a multilevel waveform
P_{cl}	[W]	Power loss due to the energy conversion process
P_{nl}	[W]	Power loss due to the no-load consumption
P_o	[W]	Output power or load power
P_t	[W]	Total inverter loss (no-load + conversion)
$\Re$	[-]	Transformer relation-ratio
$\Re(t)$	[-]	Instantaneous equivalent relation ration
$\Re_{pk}$	[-]	Peak value of the equivalent relation ration
$\Re_n$	[-]	Physical relation ratio between transformer primary and the n^{th} secondary coil
R_1	[Ω]	Resistance of transformer primary (transformer model)
R_2	[Ω]	Resistance of transformer secondary (transformer model)
R_{ds}	[Ω]	Static drain-to-source on-resistance of a MOSFET
R_{eq}	[Ω]	Single equivalent primary resistance
R_m	[Ω]	Resistance that model the core loss (transformer model)
R_n	[Ω]	Designator of the snubber resistors of the n^{th} output cell
R_w	[Ω]	Equivalent resistance of the voltage source and wires
S_x	[-]	Designator of the H-bridge switch modules (x = a,b,c,d)
S_n	[-]	Designator of n^{th} output-stage switch module

$S_{n/x}$	[-]	Designator of n^{th} output-stage MOSFET (x = a,b)
t	[s]	Time
T_c	[s]	Controller control-period
T_j	[ºC]	Junction temperature
T_z	[s]	Hold-on-at-zero interval
V_{AC}	[V]	RMS value of an AC voltage
V_b	[V]	Resulting battery voltage after input front-end
V_{bat}	[V]	Battery voltage
V_{ce}	[V]	Collector-to-emitter voltage of a IGBT (in conduction)
V_{DC}	[V]	Average value of a voltage waveform
V_{ds}	[V]	Rated drain-to-source voltage of a MOSFET (breakdown)
V_{in}	[V]	Voltage at inverter input terminals
V_{ip}	[V]	Transformer internal voltage (primary)
V_n	[V]	Nominal voltage of the n^{th} secondary coil
V_o	[V]	Output voltage (after the filter, before protections)
V_{os}	[V]	Output-stage voltage
V_{ospk}	[V]	Peak value of the output-stage voltage
V_{out}	[V]	Voltage at inverter output terminals
V_p	[V]	Transformer primary voltage
V_{pn}	[V]	Partial voltage across the n^{th} cell of the output-stage
V_{pk}	[V]	Peak value of a voltage waveform
V_{RMS}	[V]	RMS value of a voltage waveform
V_{sn}	[V]	Voltage across the n^{th} switch
Z_n	[Ω]	Designator of the zenner diodes of the n^{th} output cell
W_p	[W]	Peak power expressed in Watts

Glossary of terms

AC	Alternating Current (AC) - usually with frequency of 50/60 Hertz
A/D	Analog to Digital
BOS	Balance of System
DC	Direct Current (DC)
DC/AC	Direct Current / Alternate Current
Genset	A generator set with a start and stop controller
Grid	Public electricity system (or utility system)
H-bridge	Well-known converter structure, composed by at least 4 switches
HF	High Frequency
HF-PWM	High Frequency - Pulse Width Modulation
HP	Horse Power (1 HP = 746 W)
ICP	In Circuit Programming
IGBT	Insulated Gate Bipolar Transistor
ISET	Institut für Solare Energieversorgungstechnik
LCD	Liquid Crystal Display
LEM	LEM NORMA GmbH - A manufacturer of current sensors and equipments
LF	Low Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracker
MTBF	Mean-Time-Between-Failures
NPC	Neutral Point Clamped (A well-known multilevel converter topology)
OrCAD	Oregon Computer Aided Design - from Cadence Design Systems, Inc.
PSPICE	Personal Computer Simulation Program with Integrated Circuit Emphasis
PV	Photovoltaic (also designates a solar module)
PWM	Pulse Width Modulation
RE	Renewable Energy
RES	Renewable Energy System
RMS	Root Mean Square
SARES	Stand Alone Renewable Energy System
SMPS	Switch Mode Power Supply
SMA	Company that manufactures inverters (SMA Regelsysteme GmbH)
Sunny Boy	Grid inverter manufactured by the company SMA
THD	Total Harmonic Distortion
THD_{xy}	Total Harmonic Distortion - calculated until the xy^{th} harmonic
UPS	Uninterruptible Power Supply
WIND	Term used to abbreviate "Wind energy system"

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1 Introduction

1.1 Evolution of electricity supply systems

Since Old Stone Age, humans have been exploring different ways to use sources of energy as a mean to improve or even keep them alive. The first discovered source of energy was the fire and its products of heat and light are useful until today.

Nowadays, electricity is recognized as the most flexible type of energy and the modern civilization is highly dependent on it. Electricity is generated and supplied to the world by two types of systems: large scale and integrated systems (utility) and small autonomous systems (stand-alone). The latter is most commonly used in rural or remote regions in which utility power is unavailable [1-4].

Electricity is so fascinating in its capability to be transported and transformed that humans have been abused of its use, resulting in congested systems and rationing programs [5-9]. Even more problematic are the environmental impact and pollution caused by the conventional[1] generating systems, in special by thermoelectric power plants which use fossil fuels or radioactive materials. Looking forward, fossil fuel reserves are limited and alternatives sources must be considered for the near future [10,11].

In response to these problems, in the last decades, utility systems have adopted the following directives:

1) To develop competitive renewable[2] energy (RE) technologies;
2) To promote the rational use of electricity;
3) To promote energy savings by management of all forms of energy;
4) To promote the distributed electricity generation by using RE.

Not only have the grid experienced an evolution. Stand-alone systems also have their concepts revised, as illustrated in figure 1.1.

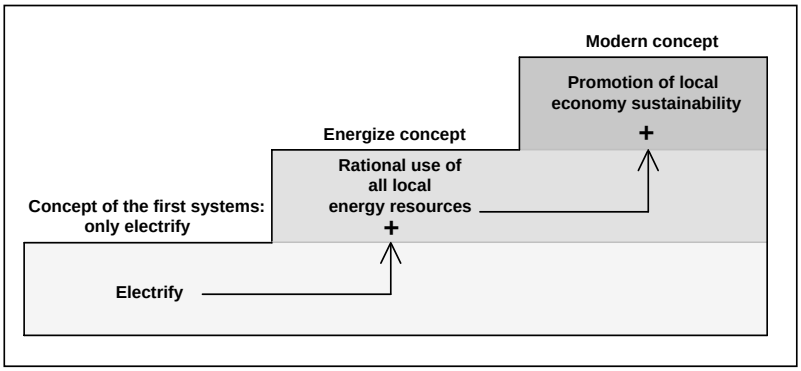

Figure 1.1 - Concept evolution of stand-alone systems.

Since most stand-alone systems are already based on RE, its evolution is based on the improvement of the social impact it causes. More than simply electrify a region, it should promote the rational use of all local energy resources and also, when applicable, use RE technologies based on natural resources that can improve the economy[3] of the region [12,13].

[1] Are considered conventional sources: fossil-fuels, nuclear, geo-thermal and large hydro-power,
[2] Are considered renewable sources: solar, wind, marine and small hydro.
[3] For example, in a region where natural source of vegetable oil is available, it could be used as combustible to feed a motor-generator instead of conventional diesel. In turn, production of the oil can also generate sub-products that can improve the local economy.

1.2 Demand on stand-alone renewable energy systems (SARES)

Currently, independently of the energy source, SARES[1] present relatively high implementation costs. In consequence and in general, SARES are applicable when utility expansion costs exceed its implementation costs. In fact, just few kilometers are enough for most cases [14-16].

Although these situations can occur in developed countries, such as houses in the European Alps, most demand is encountered in the developing countries. It is estimated that 2 billion of people are living without connection to the electricity grid and this amount is increasing [17].

Despite of SARES size, location and explored RE resource, it is of common sense that it should be capable to supply alternating current (AC) electricity[2] [18], thus providing compatibility with standard appliances that are cheap and widely available. On the other hand, most SARES include at least one DC voltage source that must be further converted into standard AC voltage source. Photovoltaic (PV) generators and most common energy storage devices[3] are typical examples of DC voltage sources. According to these facts, it is evident that a device capable to convert DC voltage in AC voltage is a key element of most SARES.

The DC/AC converters, commonly referred as inverters, have experienced great evolution in the last decade due to its wide use in uninterruptible power supplies (UPS) and industry applications. However, it is still a critical component to most SARES and the development of high performance[4] inverters is even today a challenge [19-21].

1.3 Inverters technologies

Inverters can be classified by their output waveform in four categories: square wave, modified square wave (also called quasi-square or modified sine wave), multilevel (or multi-step) and sine wave (synthesized from a high frequency pulse width modulation - PWM). Figure 1.2 shows the waveforms for each category.

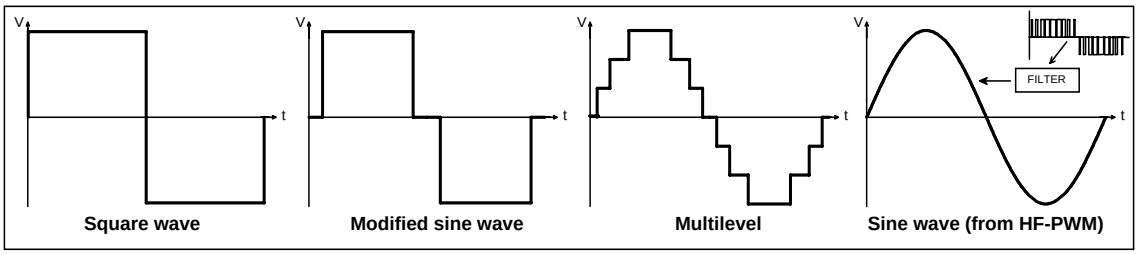

Figure 1.2 - Waveforms of different inverters technologies.

Although the square wave and the modified sine wave inverters can be acceptable in some practical applications, and are still available in the market, they are not recommend to new designs due to its very poor quality waveform.

Multilevel and sine wave inverters are considered the state of the art technology and several topologies are used to implement them. What mainly differs multilevel from sine wave inverters is the switching frequency. The former is based on low frequency switching while the latter is based on high frequency switching.

[1] In this work, it is considered systems for general purpose applications, where the load nature can be diverse, subjected to changes or not precisely defined.
[2] Standard AC voltage used in utility distribution systems. Frequency and voltage can vary from country to country. Typical voltages are 110, 115, 120, 220, 230 and 240 V_{AC}. Frequencies are worldwide fixed in 50 Hz or 60 Hz.
[3] The most commonly energy storage devices used in SARES are batteries and full-cells.
[4] In terms of reliability, efficiency, surge power and cost.

While for high[1] power applications multilevel inverters are the best available alternative, for medium or low power applications a controversy takes place. Experts on high frequency converters point out the compactness and reduced cost that can be achieved by employing high frequency switching [22-24]. On the other hand, experts on low frequency converters claim that the very best efficiency and robustness belong to the topologies based on low frequency switching [25-28].

In fact, decision about what topology is better depends on the application and moreover on the parameters used to define the performance criteria. In the particular case of SARES, the most important performance parameters are reliability, surge power capacity and efficiency. Consequently, multilevel inverters present great potential for such applications and have gained attention of recent works [29-32].

Perhaps, in the future, inverters could become obsolete devices and revolutionary technologies will give origin to current unimaginable new topologies. But while this scenario does not take place, the best should be done: work on high performance technologies.

1.4 Objectives and chapter organization

The main objectives of this work are:

- To study, design and implement a multilevel inverter, based on the multi-winding-transformer topology, using state of the art components;
- To show that the multi-winding-transformer topology is one of the best alternatives to implement inverters for SARES applications.

In chapter 2, typical SARES configurations are presented and it is identified what inverter characteristics are necessary to attend these applications. Chapter 3 makes short review about multilevel inverters and shows which topologies are more suitable to implement inverters for SARES applications. In chapter 4, the analysis, design and simulation of the proposed inverter are presented and the implemented prototype is detailed in chapter 5. Chapter 6 presents experimental results and the characteristic curves of the implemented prototype are presented. Performance analysis and cost evaluation of the proposed inverter are realized in chapter 7. Finally, conclusions, relevant contributions and future work are presented in chapter 8.

[1] High power: > 1 MW.

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2 Load profile, system configurations and inverter specification

The current demand on high-performance inverters for stand-alone applications can be reached by an optimized design that is in accordance to the load profile and system configuration of typical RES. In addition, characteristics such reliability, surge power capacity and efficiency are important specifications that must be considered in the inverter design.

2.1 Load profile

Two main parameters of the load profile that affects inverter specification are the peak demand and surge power. While the peak demand is easily estimated by simply summing the nominal power of all consumer appliances (worst case), estimation of surge power is difficult because many appliances do not have information about their startup transient. Common examples are refrigerator and water pump that usually employ single-phase induction motors, which present startup current of several times of their respective rated value [33].

For example, the average consumption of a rural property in Brazil has been estimated to be 45 kWh/month with surge power of 5 kW [34]. Considering that all consumption occurs within 2 hours in a day (optimistic supposition), then the peak power demand is equal to 750 W. In close, this application may require an inverter that should be capable to provide 750 W continuously and 5000 W of surge power, which will supply an average load demand of 63 W. This example makes clear that high performance inverters must present high surge power capacity and low stand-by consumption.

Another load characteristic that must be observed is the energy distribution as a function of the delivered power. Figure 2.1 shows a typical example of such characteristic [35].

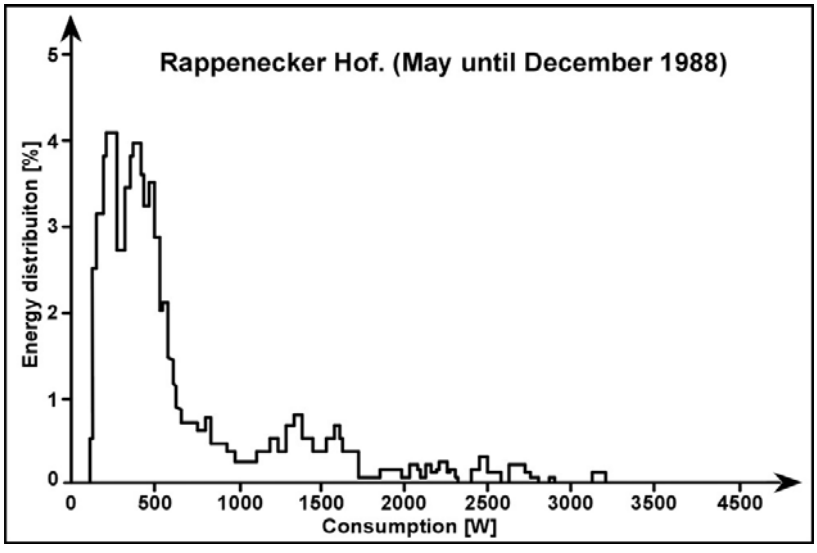

Figure 2.1 - Load profile of a typical stand-alone system (Rappenecker Hof [35]).

As can be seen in figure 2.1, if an inverter is used to feed this consumer, it will process most energy at a fraction of its nominal power; thus its efficiency characteristic must be optimized in the low load region, even if this implies in efficiency reduction at rated power.

2.2 System configurations

SARES range in size from small dedicated systems that provide few W_p, to complex mini-grid[1] systems with peak capacities of more than a MW_p. Most single consumer applications require up to some kW_p and a variety of system configurations are commonly used to implement them [10,36].

2.2.1 *Single source systems*

Figure 2.2 shows a typical single source system, composed by a PV system with battery backup.

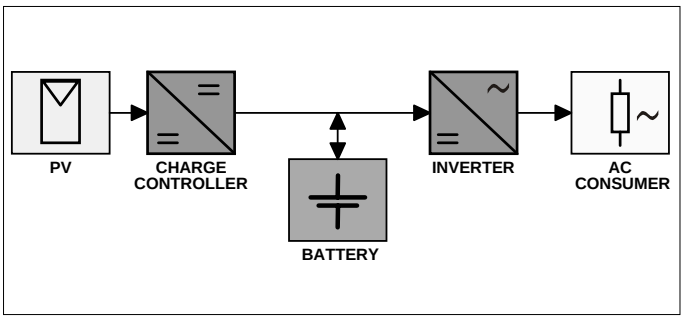

Figure 2.2 - Typical single source system.

As in the example illustrated in figure 2.2, due the intermittent nature[2] of almost all RE sources, most single consumer SARES include an energy storage device that is usually implemented by lead-acid battery banks [37-39].

The required inverter is fed directly by the battery bank, which usually present a DC voltage in the range from 12 V_{DC} to 96 V_{DC}.

2.2.2 *Multiple source systems (Hybrid systems)*

Hybrid systems are those supplied by at least two different energy sources [40-42]. In many applications, a motor-generator set (genset) is combined with one or more RE source, as shown in the example of figure 2.3. In practice, hybrid systems enjoy a high degree of reliability as compared to single source systems.

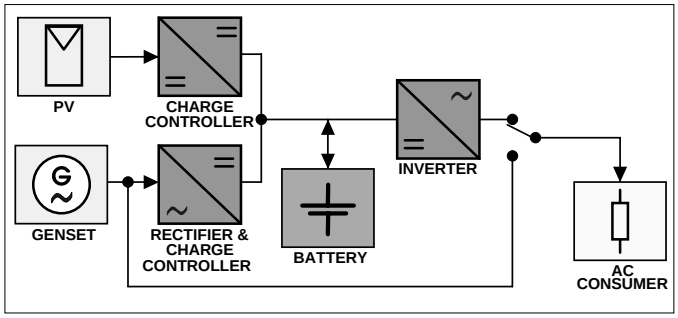

Figure 2.3 - Conventional hybrid system.

In the conventional system shown in figure 2.3, the inverter is disconnected from the load while the generator is running. Thus, it requires a simply battery inverter like the single source configuration.

[1] Mini-grids are larger SARES that combines several generators (usually distributed) in order to form a small grid.
[2] Several RE sources are highly intermittent, such as solar and wind energy. Several others can be seasonal, including small hydropower, biomass and marine waves. Exceptions are geothermal and marine tide, which can present continuous or almost continuous capacity, respectively.

A variation of the conventional hybrid system is shown in figure 2.4, where the inverter is bi-directional[1] and can be connected in parallel with the generator [10,43]. In this case, use of a bi-directional inverter make possible to reduce the number of components of the system.

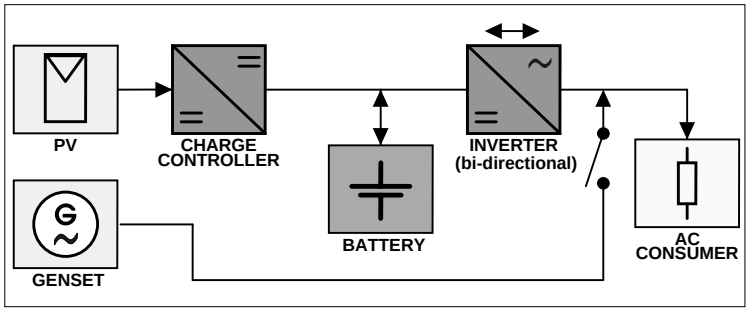

Figure 2.4 - Variation of the conventional hybrid system (Using a bi-directional inverter).

Other two configurations are shown in figure 2.5.

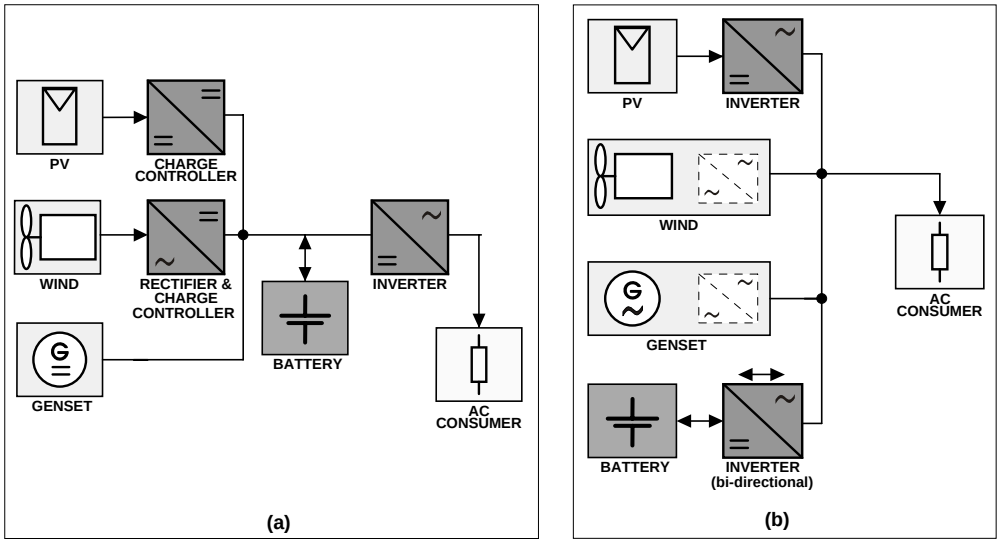

Figure 2.5 - Modular hybrid systems: (a) DC bus modular system; (b) AC bus modular system.

The configurations shown in figure 2.5 are modular and can be easily expandable to incorporate new power sources or even to compose a mini-grid system. Advantages and disadvantages of each configuration are discussed in [43]. Related to the inverter, it should be noted that:

1) in the DC bus configuration, the inverter must be very reliable because it is the only alternative to generate regulated output AC voltage;

2) in the AC bus configuration, the most critical inverter is the battery inverter because the other modules, except for the generator, usually are not projected to support surge power demand. This battery inverter could not be bi-directional, but, in this case, an additional battery-charger module is required.

[1] Power can flow in both directions: from the DC side to the consumer side (inverter operation) and from de AC side to the battery (battery-charge-mode).

2.3 Inverters for SARES applications

Parameters such as voltage and frequency regulation, total harmonic distortion and operation temperature, among others, can be considered as standard specifications[1] that are matched by all high quality inverters present in the current market [44-50]. On the other hand, besides device cost, performance parameters[2] and extra features[3] have been used to specify an inverter according to each specific application.

Having in mind that SARES only make sense if they can be reliable and flexible, then all balance of system (BOS) components must accomplish with these characteristics. In this way, from the best of the author's knowledge, the most important characteristics of a RES inverter, in order or importance, are:

1) Reliability (most important);
2) Surge power capacity;
3) No-load consumption and efficiency.

In the following sections, each characteristic is discussed in detail.

2.3.1 *Reliability*

Reliability is the probability that a device or system will perform its specified function in a given environment for a specified period of time. Traditionally, reliability of a system have been presented in terms of Mean-Time-Between-Failures (MTBF) and it is usually modeled by a Bathtub curve[4] [51-54].

Although inverters have experienced great evolution in the last decade, even today they still have the bad reputation to be considered one of the most critical BOS of a RES [19,55]. In the particular case of PV RE systems, in which PV modules can have an expected lifetime of 25 years [52,56,57], inverters can be considered the most critical component.

In the last years, in response to the actual demand on RES quality and increasing market competition, reliability concerns have gained more attention from inverter manufactures. Nevertheless, while standard warranty up to 10 years are offered for grid inverters [58,59], manufactures are still timid to talk about expected lifetime of their stand-alone inverters [44-50]. This fact shows how these components are critical and demand further improvements.

It is well know that voltage stress and high temperature are factors that decrease semiconductor lifetime [60,61]. Taking this into account, it is expected that high efficiency (therefore less heat and lower temperature) and stable (therefore less or more predictable voltage stress conditions) topologies, like multilevel topologies, can reach high degree of reliability.

2.3.2 *Surge power capacity*

Systems capable to start a refrigerator or a conventional water pump are undoubtedly more useful than systems that can supply only well-behaved devices, such as lights, radio and television. This is why surge capacity can be considered the second most important inverter feature.

---

[1] There is lack of standards for RES inverters. Therefore, some specifications, such as maximum voltage THD of 5%, have been widely accepted and are copied from diverse other standards.
[2] Some are: reliability, efficiency, surge power capability and degree of protection: in order of importance.
[3] For example: communication features, operation modes and utility interaction capability.
[4] The Bathtub curve plots the failure rate over time and it is divided in three intervals that are modeled by three distinct Weibull distribution functions.

In general, for the same cost-benefit relation, inverters based on low-frequency switching present higher surge power capacity when compared to similar products based on high frequency switching. In fact, current available HF-PWM inverters usually present surge power around twice their rated power while low frequency inverters can easily present more than three times [44-50].

2.3.3 *Efficiency characteristic*

Efficiency characteristic is directly related to inverter cost and system overall efficiency, and also indirectly related to system reliability (higher efficiency usually implies in lower working temperature and stress) and durability (for example, lower losses can result in less deep battery discharge).

Regarding cost, trade-off between efficiency characteristic and inverter cost exists. For example, the use of switches of better performance and transformers with better core materials can improve efficiency characteristic at the expense of higher cost.

Regarding system overall efficiency, influence of the inverter efficiency characteristic depends on the load profile. Moreover, inverter efficiency characteristic must include both information about no-load consumption and efficiency versus power curve. All these information must be available in order to determine the real inverter performance.

To analyze an inverter performance, it is convenient to model the inverter efficiency characteristic by its no-load consumption (P_{nl}) and conversion efficiency (η_c) curve. Figure 2.6 shows how to calculate the equivalent conversion efficiency for a given conventional efficiency point.

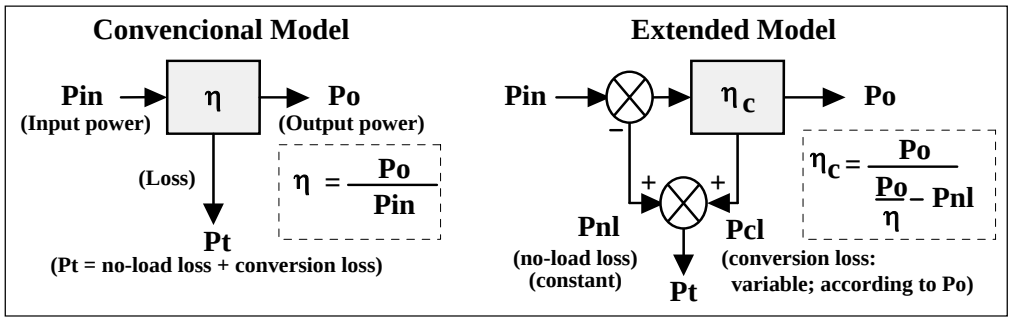

Figure 2.6 - Conversion between conventional model and extended model.

As can be seen in figure 2.6, the extended model separates the no-load consumption from the conversion process. In consequence, for a given load profile, an inverter can be fully characterized by only two parameters: its no-load consumption and its mean weighted conversion efficiency (η_{cw}). The η_{cw} is the mean value of the weighted η_c curve (weighted by the load profile), and can be calculated by equation 2.1.

$$\eta_{cw} = \frac{\int \eta_c(P_o).L_p(P_o).dP_o}{\int L_p(P_o).dP_o} \qquad (2.1)$$

As an example, using an approximation of the load profile given in figure 2.1, the calculated η_{cw} and respective efficiency curves (conventional and conversion) of a LF-based inverter (inverter-1) and HF-based inverter (inverter-2) are shown in figure 2.7.

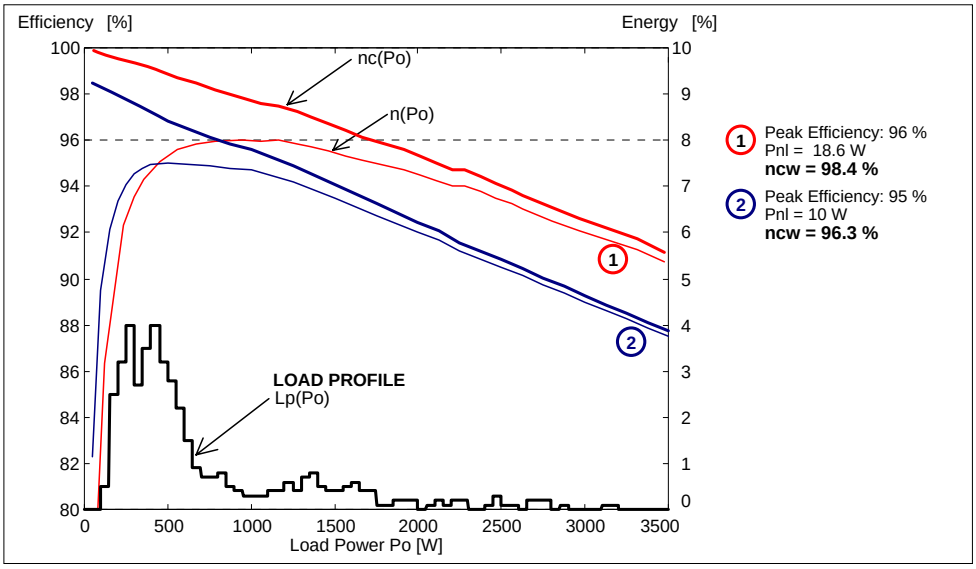

Figure 2.7 - Load profile and efficiency characteristic of two different converters.

From the data presented in figure 2.7, it is possible to note that:

1) Although inverter-1 peak efficiency is only 1% higher than inverter-2, it is 2.1% more conversion-efficient for the given load profile.
2) The conversion efficiency versus power characteristic can be approximated by a straight line. This fact suggests that the efficiency characteristic of an inverter can be completely described by only 3 numbers: its no-load consumption and the two coefficients of the line that better fits the η_c curve.
3) The conversion efficiency curve of inverter-1 approximately converges to the value of 100 %, while the inverter-2 characteristic converges to a value between 98 % and 99 %. This difference can be justified by the fact that inverter-1 is based on low-frequency switching and inverter-2 is based on high-frequency.

In practice, according to the inverter usage, such differences imply in distinct performances, as shown in figure 2.8.

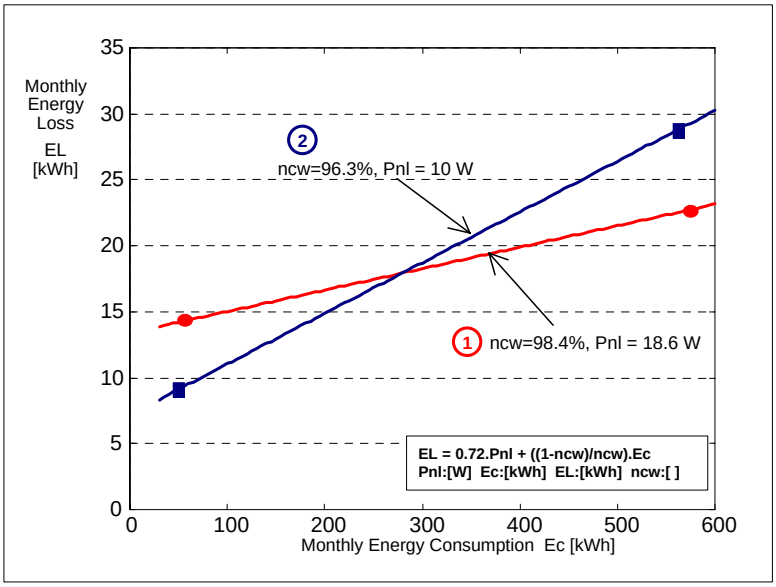

Figure 2.8 - Monthly energy loss versus processed energy.

As can be seen in figure 2.8, inverter-2 presents lower losses for any energy demand of up to approximately 270 kWh/month (average: 375 W), and above this value inverter-1 is more efficient.

In fact, performance of two inverters can be compared easily by using the graphic shown in figure 2.9. For this example, the relation between no-load consumption and conversion efficiency variations is equal to 4.1 W/% (8.6/2.1) and the product of their conversion efficiency is 0.95 (0.984*0.963). Using these data in figure 2.9, it is found that both inverters present same energy losses at about 270 kWh/month, and the inverter with lower no-load consumption will present lower losses for energy demand lower than this value.

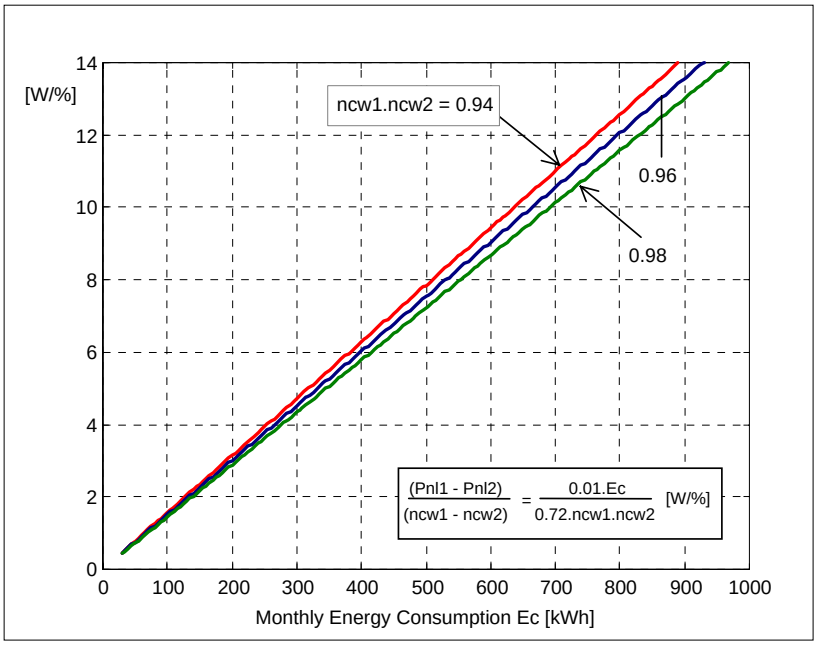

Figure 2.9 - Relation ratio between no-load-consumption and efficiency variations for inverters with same losses, as a function of the energy demand.

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3 Multilevel topologies

It is a fact that, until today, multilevel topologies are the best alternative to implement low-frequency based inverters with low output voltage distortion. This chapter makes a review about most common multilevel topologies and shows which ones are more suitable to implement inverters for SARES.

3.1 The multilevel concept and notation.

A multilevel inverter can be defined as a device that is capable to produce a stepped waveform. The generalized stepped waveform is shown in figure 3.1.

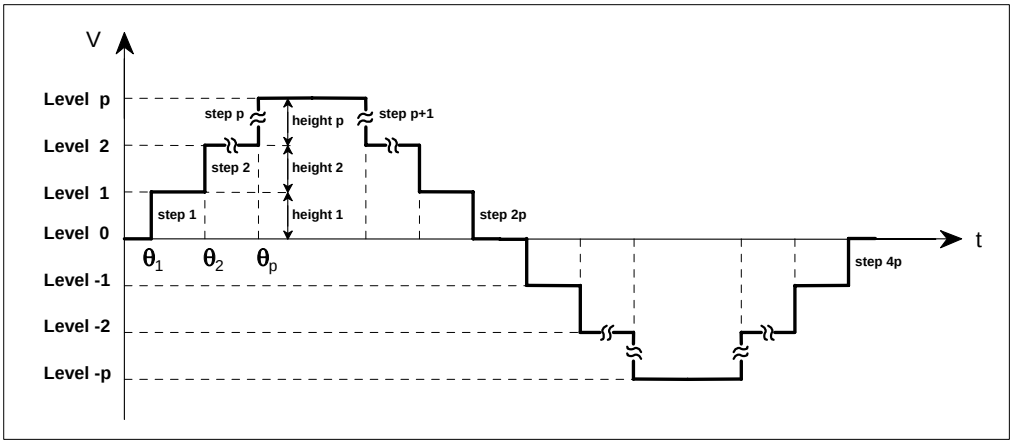


Figure 3.1 - Generalized stepped waveform.

Usually, and also in this work, the follow definitions apply:

p: number of steps in a quarter-cycle;
2*p + 1: number of levels of a converter;
4*p: number of steps of a converter.

In the generalized waveform, both width and heights of the steps can be adjusted. However, heights of steps are usually made equal and only widths are adjusted according to the desired waveform shape. It this case, a multilevel waveform is fully characterized by its p switching angels (θ_1, θ_2 ... θ_p) [62, 63].

Because any practical multilevel voltage waveform is composed by a finite number of levels, it is important to consider that its peak may differ from the value calculated from its RMS value. Such difference can be quantified by the modulation index (M_i) defined by equation 3.1.

$$M_i = \frac{\left(V_{pk} / \sqrt{2}\right)}{V_{RMS}} \qquad [-] \qquad (3.1)$$

where: V_{pk} and V_{RMS} are the peak and RMS value of the waveform, respectively.

More than a quality parameter, if the number of levels of a multilevel waveform is fixed (fixed V_{pk}), then M_i can be used as a measurement of voltage regulation.

3.2 Application field and trends

Multilevel converters have been mainly used in medium or high power systems applications, such as static reactive power compensation and adjustable speed drives [64-68]. In these applications, due limitations of current available power semiconductor technology, multilevel concept are usually the unique alternative because it is based on low frequency switching and also provides voltage and/or current sharing between power semiconductor switches [69-72].

On the other hand, for small power systems (<10 kW), multilevel converters have been competing with high frequency PWM converters in applications where high efficiency is of major importance. Moreover, lower prices of power switches and new semiconductor technologies, as well as the current demand on high performance inverters required by RE systems, have extended the applications of multilevel converters [29-32].

3.3 Multilevel inverter topologies

Several topologies are available to implement multilevel converters. In this section, short review of most common topologies are presented.

3.3.1 *Neutral point converter (NPC) / Diode-clamped topology*

Proposed by Nabae et al. (1981), the inverter shown in figure 3.2 is called as three-level NPC inverter [73]. It was the first widely popular multilevel topology and it continues to be extensively used in industry applications. Later, the NPC inverter was generalized for a greater number of levels, using the same concept of diode-clamped voltage levels, what resulted in the current designation of diode clamped converter [74].

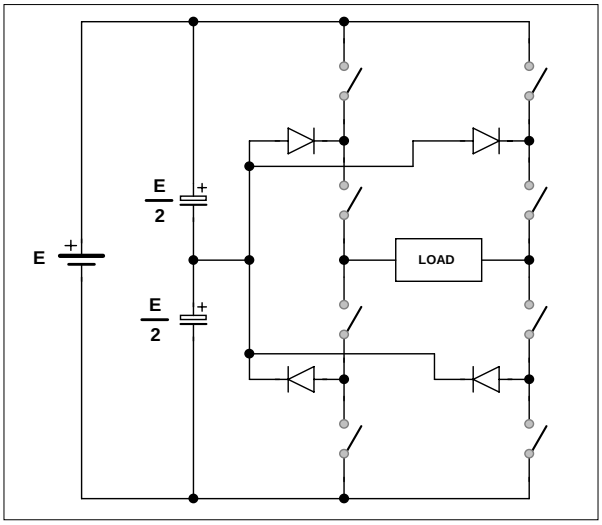


Figure 3.2 - Diode clamped topology (p = 3).

As can be seen in figure 3.2, the 3-levels NPC inverter uses capacitors to generate an intermediate voltage level and voltages across the switches are only half of the DC input voltage. Due to capacitor voltage balancing issues, practical diode-clamped inverters have been mostly limited to the original 3-level structure [53,75,76].

3.3.2 *Flying capacitor*

The three-level flying capacitor topology, shown in figure 3.3, can be considered a good alternative to overcome some of the NPC topology drawbacks [77,78].

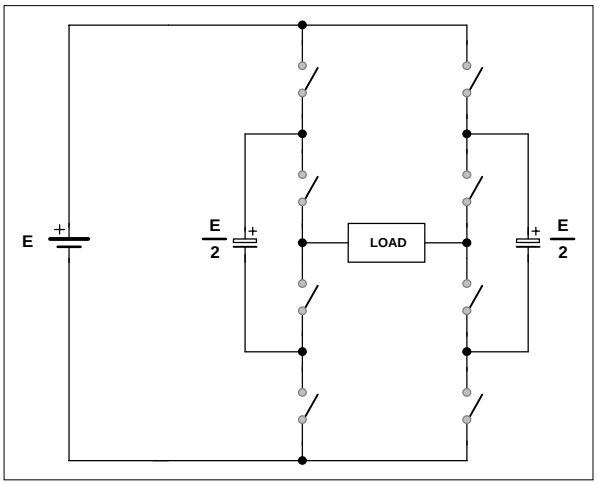


Figure 3.3 - Flying capacitor topology (p = 3).

In this topology, additional levels and voltage clamping are achieved by means of capacitors that "float" with respect to the DC source reference. It does not require additional clamping diodes and also provides redundant switch states that can be used to control the capacitors charge even under loads with DC level [79]. Nevertheless, larger structures require relatively high number of capacitors and additional circuits are also required to initialize capacitors charge.

3.3.3 *Cascaded H-bridge (or cascaded inverter)*

This topology is composed by several H-bridge (also referred as Full-bridge) converters in a cascade connection. Figure 3.4 shows a 3-cell cascaded inverter.

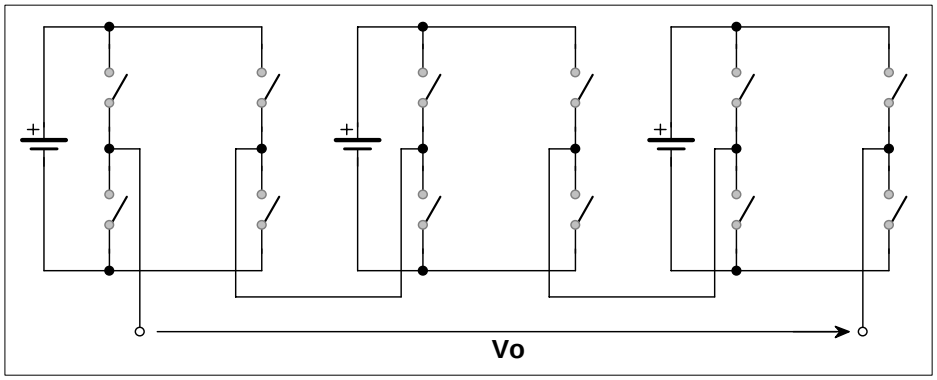


Figure 3.4 - Cascaded H-Bridge (three-cell)

The cascade topology allows the use of DC sources with different voltage values and high resolution multilevel waveforms can be achieved with relatively low number of components [80-83]. In addition, DC sources can be added or subtracted, what can increase the number of output levels.

Although this topology requires isolated DC sources, in some systems they may be available through batteries or photovoltaic panels, and it has been used to implement high efficiency transformer-less inverters [84]. When AC voltage is already available,

multiple DC sources can be generated using isolation transformers and rectifiers. If only one DC source is available, then it is possible to use the topology shown in figure 3.5 [85].

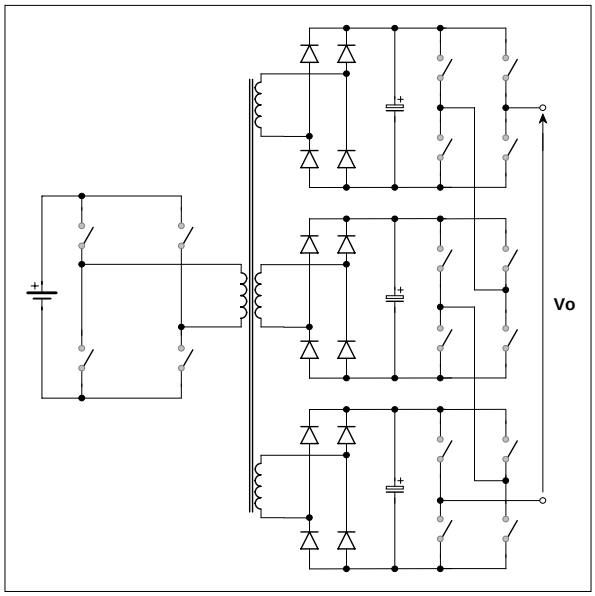


Figure 3.5 - Cascade H-Bridge with multi-winding transformer.

The topology shown in figure 3.5 is simple but losses in additional rectifier diodes can be significant and it does not support bi-directional power flow. These problems are overcome by using the topology shown in figure 3.6 [86].

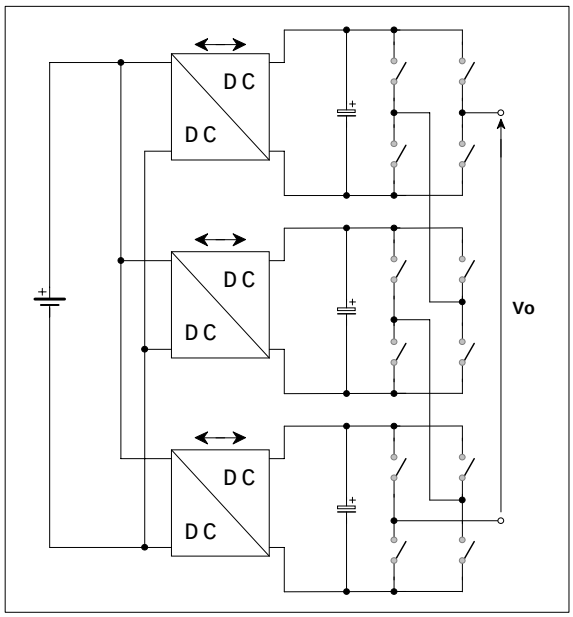


Figure 3.6 - Cascade H-Bridge with bi-directional DC/DC converters.

The topology shown in figure 3.6 can be very efficient if soft-switching DC/DC converters are used [29]. On the other hand, this topology is based on high-frequency switching and inherent benefits of low frequency switching are lost.

3.3.4 *Multiple-transformer topology*

Figure 3.7 shows a multiple transformer topology composed by three cells. It is similar to the cascaded H-bridge topology, but the output of the isolation transformers are cascaded instead of cascading directly the H-bridge outputs. As a result, all H-bridge can be referenced to a same point and only one DC source is required.

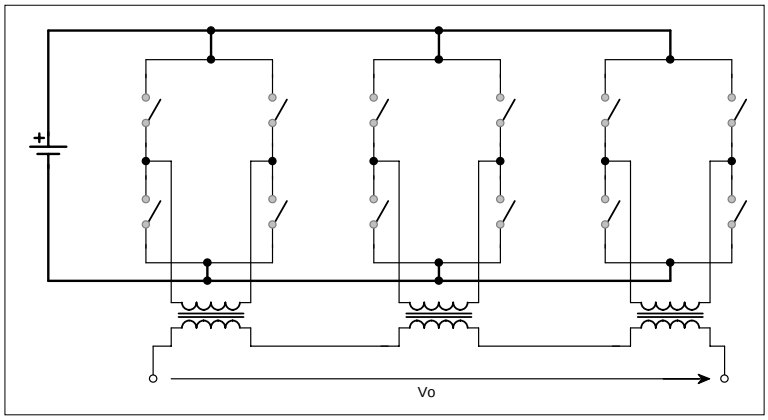


Figure 3.7 - Cascade H-bridge with several isolation transformers.

Currently, there are available in the market some commercial inverters (for SARES applications) that are based on this topology [44,48]. In practice these inverters have been proved to be very robust and reliable. One disadvantage of this topology is the fact that it requires several low frequency transformers.

3.3.5 *Multiple-source topology*

The multiple-source topology, shown in figure 3.8, uses several isolated DC sources to produce a rectified multilevel waveform which is latter converted in an AC multilevel voltage [10,87].

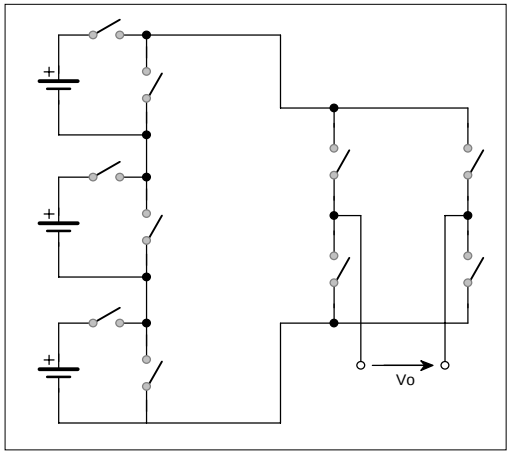


Figure 3.8 - Multiple-source topology.

In practice, the multiple-source topology is one of the most efficient multilevel topologies currently available. It has been tested in some RES for more than 10 years and it has proved to be very efficient, robust and reliable [88]. The disadvantage of this topology is the fact that it requires several isolated DC sources and do not provide input-output isolation.

3.3.6 *Multi-winding-transformer topology (adopted topology)*

The multi-winding transformer topology can be considered as a variation of the multiple-source topology. A three-cell multi-winding inverter is shown in figure 3.9.

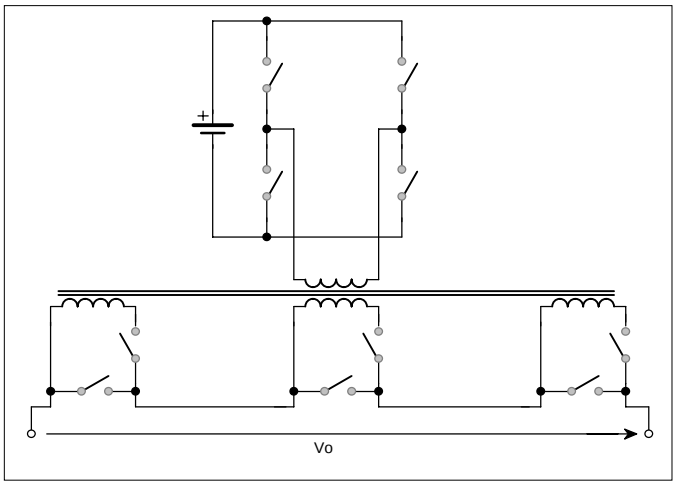


Figure 3.9 - Multi-winding-transformer topology.

Unlike the multiple-source topology, it operates with a single DC input, what is achieved by the use of a multi-winding line-frequency transformer. It provides input-output isolation and, because it employs only one transformer, high efficiency can be achieved. The major disadvantage is the relatively high number of switches presented in the output stage. This is the topology adopted in this work.

3.3.7 *Modular topology*

Figure 3.10 shows an eight-module modular topology that was recently proposed for high power applications [89,90].

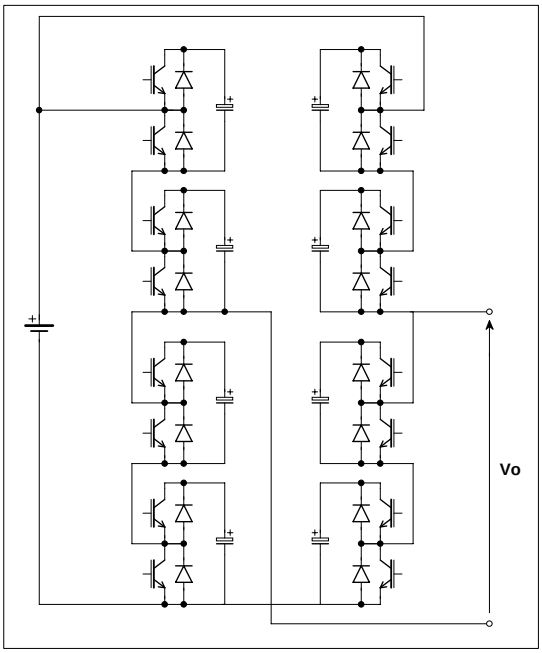


Figure 3.10 - Modular topology (eight-module).

This topology is highly modular and each module is a two-terminal device composed by two switches and one local DC-storage capacitor. As disadvantages, it requires a voltage measurement circuit for each module capacitor and it does not support loads with DC current component.

3.3.8 *Hybrid converter topology*

The hybrid term is not associated to any specific topology, but it refers to the converters which operate with both high and low frequency switching [71,91].

3.4 Selection and comparison of topologies

As discussed in chapter 2, most SARES systems require a single input battery inverter with improved characteristics of reliability, surge power capability and efficiency. In addition, such kind of inverter must be capable of work with loads of diverse nature, such as house appliances, and thus must produce an output voltage with acceptable waveform quality. Taking into account these requirements, a list of basic characteristics and respective priorities was defined (arbitrary), as presented in table 3.1.

Table 3.1 - List of basic specifications required by a high-performance battery inverter topology.

Id.	Inverter characteristic	Priority
M1	Single source input	Mandatory
M2	Mainly based on low-frequency switching	Mandatory
M3	Capable to feed loads with DC level component	Mandatory
M4	Suitable to implement high-resolution multilevel waveform	Mandatory
A1	Bi-directional (4-quadrant operation)	Additional
A2	Input-output isolation	Additional

According to Table 3.1, the characteristics of all previously presented topologies are summarized in table 3.2.

Table 3.2 - Characteristics summary of most common multilevel topologies.

Topology	Fig.	M1	M2	M3	M4	A1	A2
Diode clamped	3.2	**Y**	**Y**	**-**	**-**	Y	-
Flying capacitor	3.3	**Y**	**Y**	**Y**	**-**	Y	-
H-bridge (isolated DC sources)	3.4	**-**	**Y**	**Y**	**Y**	Y	-
H-bridge (+ multi-winding transformer)	3.5	**Y**	**Y**	**Y**	**Y**	-	Y
H-bridge (+ isolated DC/DC converters)	3.6	**Y**	**-**	**Y**	**Y**	Y	Y
Multiple transformer	3.7	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**
Multiple source	3.8	**-**	**Y**	**Y**	**Y**	Y	Y
Multi-winding transformer	3.9	**Y**	**Y**	**Y**	**Y**	**Y**	**Y**
Modular	3.10	**Y**	**Y**	**-**	**Y**	Y	-

"Y": Yes, available. "-": Not available.

As can be seen in figure 3.2, only 3 topologies attend all mandatory characteristics. While multiple transformer and multi-winding transformer topologies attend all characteristics, the H-bridge topology with multi-winding transformer does not support full 4-quadrant operation.

In order to better compare these topologies, it is considered the design of inverters with minimum p = 12 (refer to section 4.7.2). It is also important to mention that the design of the H-bridge and multiple-transformer topologies may include subtraction of voltages. Both designs were considered for the multiple-transformer topology but only

addition of levels was considered for the H-bridge (because it is not bi-directional, what could result in capacitors oversize). Table 3.3 shows the achieved design data and expected performance for the selected topologies.

Table 3.3 - Design data and expected performance for equivalent inverters (minimum p = 12).

	H-bridge with multi-winding	Multiple-transformer/3	Multiple-transformer/4	Multi-winding
Number of cells	4	3	4	4
Maximum p	15	13	15	15
Power transformers	1	3	4	1
Power switches	20	12	16	20
Capacitors	4	0	0	0
Diodes	16	0	0	0
Isolated drivers	8	0	0	8
Reliability	Medium	High	High	High
Surge power capability	High	High	High	High
Conversion efficiency	Medium	Medium	Medium	High
No-load consumption	Medium	Medium	Medium	Medium
Market competitiveness	Medium	High	Medium	Medium

It is important to note that evaluation of the expected performance parameters took into account the following:

- Reliability of the H-bridge inverter was lowered because of the presence of capacitors (usually, of electrolytic type) that must support all reactive power of inductive loads;
- Conversion efficiency of the H-bridge inverter is limited by the rectifier diodes;
- Conversion efficiency of the multiple-transformer/3 inverter is limited by the subtraction of levels and also by the use of several transformers. In addition, each transformer always carries total current at any instant;
- Conversion efficiency of the multiple-transformer/4 inverter is limited by the use of several transformers, and each transformer always carry all the load current at any time;
- Conversion efficiency of the multi-winding transformer inverter is considered high because it uses only one transformer and the load current is shared between transformer output coils and switches;
- Market competitiveness of the multiple-transformer/3 inverter is considered high because additional cost of the several transformers is compensated by the cost reduction provided by its reduced number of power devices and drivers.

The presented analysis shows that the multiple-transformer and multi-winding transformer topologies are the most suitable to implement high-performance battery inverters. It is also expected that the multi-winding transformer topology can achieve better efficiency than the multiple-transformer one if same rules and similar components are used in their design. Regarding cost, it is expected that a multiple-transformer inverter can present slightly lower production cost when compared to a similar multi-winding transformer inverter. Nevertheless, the better efficiency characteristic of the latter can justify the low cost difference.

4 Study of the proposed topology, prototype design and simulation

In this chapter, the proposed topology is discussed in depth and details of practical design and optimizations are also accessed. Simulations are presented and they show some peculiar characteristics of the proposed inverter.

4.1 The proposed topology structure

As shown in figure 4.1, the proposed topology includes 3 main components: one H-bridge converter, one multi-winding transformer and one output-stage. The H-bridge converter receives voltage from a DC source, such as a battery bank, and generates a square waveform at line frequency that is applied to the primary of the transformer. The transformer operates at line frequency and it has one primary and several output coils. These coils are electrically isolated from each other, thus producing several partial AC square waveforms. The output-stage combines these partial voltages in order to produce the final output voltage.

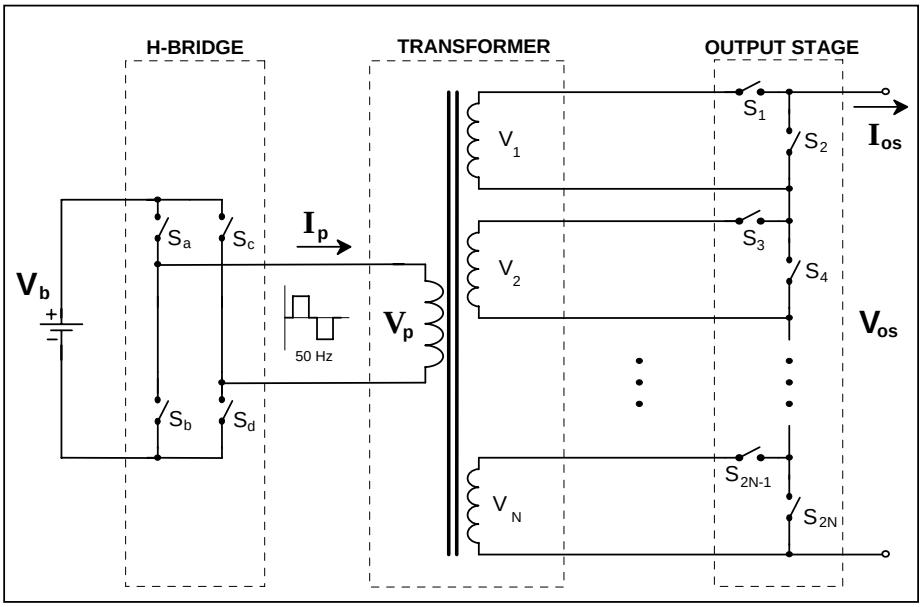


Figure 4.1 - The proposed topology.

The switches that compose the H-bridge converter must be capable to block voltages at one polarity only, and can be implemented by MOSFETs or IGBTs. On the other hand, all the switches that compose the output-stage must be capable to block AC voltage and their practical implementation is discussed in section 4.6.2.

The number of levels that can be generated depends on the number of output-stage cells and also on their respective values. For a structure composed by N cells, the maximum number of levels (same polarity) that can be produced is 2^N (including the zero). This condition is achieved if all output-coil voltages are of distinct values and if the set of possible combinations do not present repeated values. In this work, each coil voltage is a successive multiple of 2 of the lowest coil voltage; thus it is possible to produce 2^N positive levels of same height.

4.2 Operation description

Without loss of generality, the operation principle of the proposed topology will be described using a structure with an output-stage composed by only two cells, as shown in figure 4.2. Bigger structures operate in the same way, despite of their higher number of components.

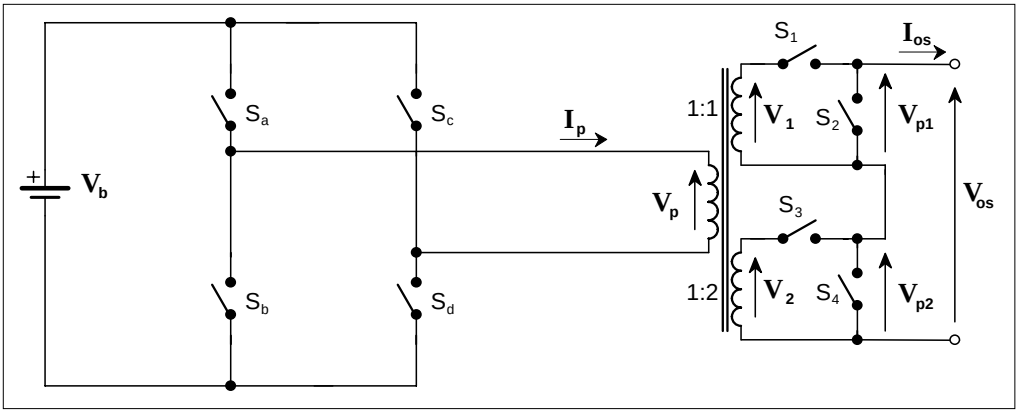


Figure 4.2 - Proposed topology: 2-cell structure.

The driver signals of all switches and main voltage waveforms are presented in figure 4.3. The H-bridge switches operate at line frequency in order to produce a square voltage waveform (V_p) that is applied to the primary of the transformer. In this example, it is used transformer relation-ratios of 1:1 and 1:2, so V_1 and V_2 are square waveforms with amplitudes of V_b and $2.V_b$, respectively.

As can be seen, each output coil is connected to two switches which operate complementarily (S_1 and S_2 for the first output-cell and S_3 and S_4 for the second one). Thus each cell produces a partial voltage that can be equal to zero or to its respective coil voltage. For example, if switch S_1 is closed and switch S_2 is opened, partial voltage V_{p1} is equal to coil voltage V_1. On the other way, if switch S_2 is closed and switch S_1 is opened, then V_{p1} is ideally zero.

As all cells are connected in series, total output voltage is equal to the sum of all partial voltages and can assume distinct values depending on the state of the H-bridge and output-stage switches. Table 4.1 resumes all possible conditions that can occur.

Table 4.1 - Output voltage V_{os} according to switch states.

S_3	S_4	S_1	S_2	V_{os} (V_p=+ V_b)	V_{os} (V_p=0)	V_{os} (V_p=- V_b)
off	on	off	on	0	0	0
off	on	on	off	E	0	-E
on	off	off	on	2E	0	-2E
on	off	on	off	3E	0	-3E

As can be seen in table 4.1, this structure is capable to produce four (2^2) distinct levels: 0, V_b, $2.V_b$ and $3.V_b$ in the positive cycle. In the negative cycle, operation occurs in the same way.

Different from other topologies, this topology can only sum partial voltages. This fact limits the maximum number of steps in 2^N - 1 (per quarter cycle). Nevertheless, this kind of operation does not include "forced reverse-power-flow" and high efficiency can be achieved.

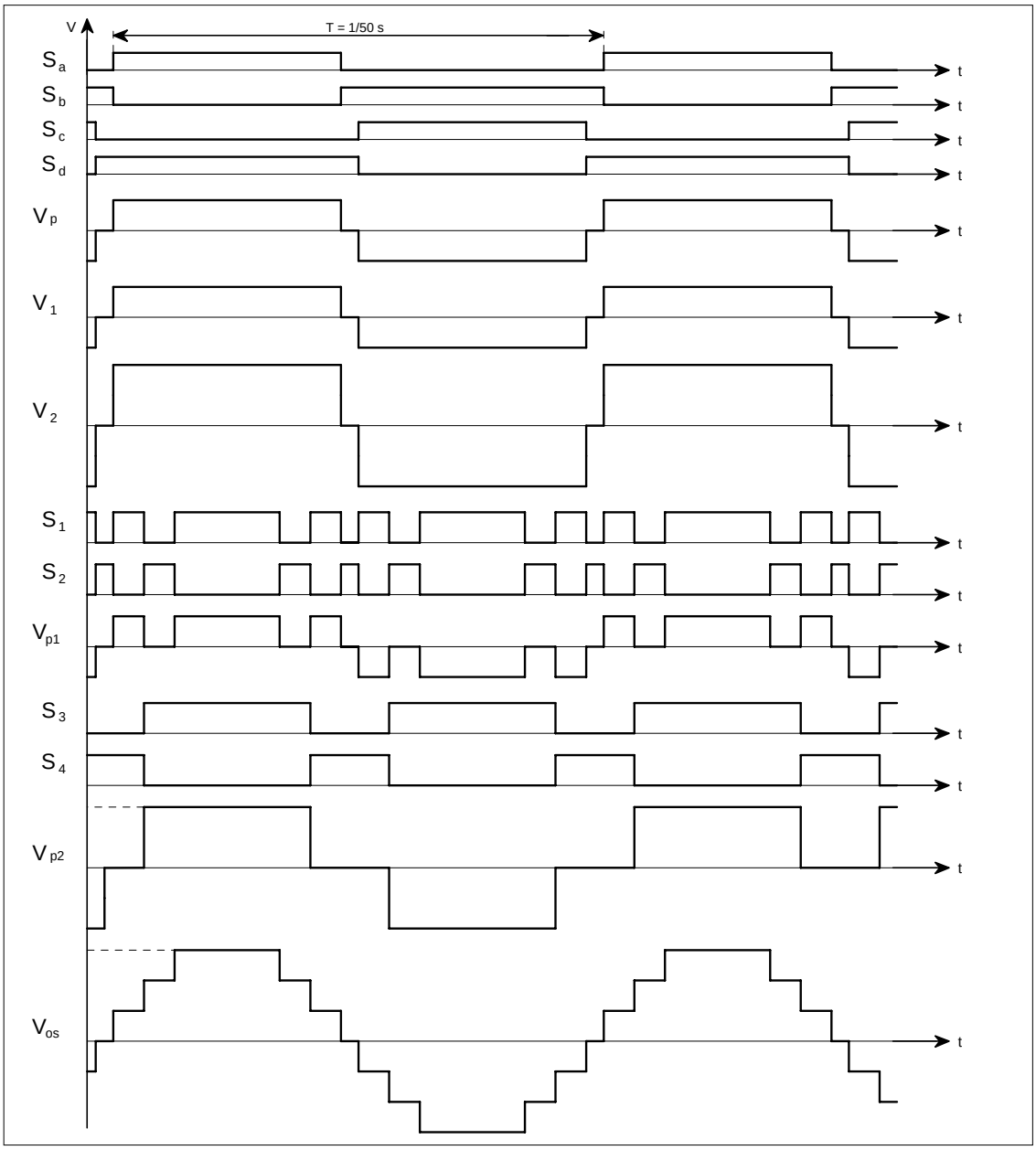


Figure 4.3 - Switch signals and voltage waveforms for a two cell structure.

Finally, it should be noted that switches of different cells operate with distinct frequencies. In fact, switches of a lower voltage cell operate with higher frequency than the switches of a higher voltage cell.

4.3 Converter equations

For a structure with N output cells organized in a binary fashion, the relation between each consecutive coil rated-voltage follows equation 4.1.

$$V_n = 2.V_{n-1} \quad , n = 2,3..N \qquad [V] \qquad (4.1)$$

where: V_n is the nominal voltage of the n^{th} coil [V].

The maximum instantaneous output voltage is equal to the sum of all partial voltages and can be calculated by equation 4.2.

$$V_{OSpk} = (2^N - 1).V_1 \qquad [V] \qquad (4.2)$$

where: V_1 is the peak voltage of the lowest voltage coil [V].

The relation between the output current and transformer input current is not easily calculated because this relation depends not only on the rated transformer relation-ratios but also depends on the output-stage state.

In fact, the transformer together with the output-stage acts as a single-output transformer with adjustable relation-ratio. In this case, the transformer primary current is determined by equation 4.3.

$$I_p(t) = \Re(t).I_{os}(t) \qquad [A] \qquad (4.3)$$

where: $\Re(t)$ is the effective relation-ratio, which is determined by the physical relation-ratios and also by the output-stage state at the instant t [-].

For an ideal case, where the converter presents an infinite number of levels, the equivalent relation-ration may be approximated by a continuous function, as given by equation 4.4.

$$\Re(t) = \Re_{pk}.|\sin(t)| \qquad [-] \qquad (4.4)$$

where: $\Re_{pk}$ is the peak value of the equivalent relation-ratio [-].

The peak value of the equivalent relation-ratio can be calculated through equation 4.5.

$$\Re_{pk} = p.\ \Re_1 \qquad [-] \qquad (4.5)$$

where: $\Re_1$ is the lowest voltage coil relation-ratio (physical, related to the primary coil) [-];
p is the number of steps in a quarter-cycle [-].

Considering the case of a resistive load, the output current is given by equation 4.6.

$$I_{os}(t) = I_{OSpk}.\sin(t) \qquad [A] \qquad (4.6)$$

where: I_{OSpk} is the peak value of the output-stage current [A].

Substituting equations 4.4 and 4.6 into equation 4.3 results in equation 4.7.

$$I_p(t) = \Re_{pk}.I_{OSpk}.\sin(t).|\sin(t)| \qquad [A] \qquad (4.7)$$

According to equation 4.7, the transformer current presents a waveform that is proportional to $\sin^2(t)$. This conclusion is important for the specification of the transformer and also for the specification of the H-bridge switches, because it allows the calculation of the RMS value, which is given by equation 4.8.

$$I_p = 0.866.\Re_{pk}.I_{OS} \quad [A] \quad (4.8)$$

where I_p is the transformer primary RMS current;
I_{OS} is the output-stage RMS current [A];
$\Re_{pk}$ is the peak value of the equivalent relation-ratio [-].

Although equation 4.8 is valid only for infinite number of levels, numerical calculations (assuming the simplified output waveform shape described in section 4.5.1) showed that, for a resistive load with p > 7, the error is less then 2%, as can be checked out in the second column of the table given in appendix A.

While the input current can be estimated by a simple analytical expression, the current through each coil and switch of the output stage can not be easily estimated. In fact, each transformer output coil does not carry all output current because there are some time periods when the output current flows through the switches (even switches).

The current share between the switches and transformer coils is strongly influenced by the effective number of levels used to construct the output voltage and also by the waveform shape. This fact can be also observed in the table presented in Appendix A, which presents all normalized currents for the case of a converter with 5 output cells, running from 7 up to 31 levels per quarter-cycle.

The switching frequency of the output-stage switches depends on the cell number and varies according to equation 4.9.

$$f_n = f_L.(2^{N - n + 2} - 2) \quad [Hz] \quad (4.9)$$

where f_L is the line frequency (in this work: 50 Hz) [Hz];
n is the number of the specific cell [-];
N is the number of cells of the inverter [-].

It is important to note that equation 4.9 assumes that the output waveform includes all possible levels. Table 4.2 shows all switching frequencies of a 5-cell inverter.

Table 4.2 - Switching frequencies for a 5-cell inverter (p = 31).

Stage	Frequency [Hz]
H-bridge	50
Cell 5 (the highest voltage cell)	100
Cell 4	300
Cell 3	700
Cell 2	1500
Cell 1 (the lowest voltage cell)	3100

4.4 Transformer-unbalancing

4.4.1 *The problem of unbalancing*

Transformer-unbalancing problem may occur due the presence of DC voltage level at its primary. Figure 4.4 shows a simplified transformer model.

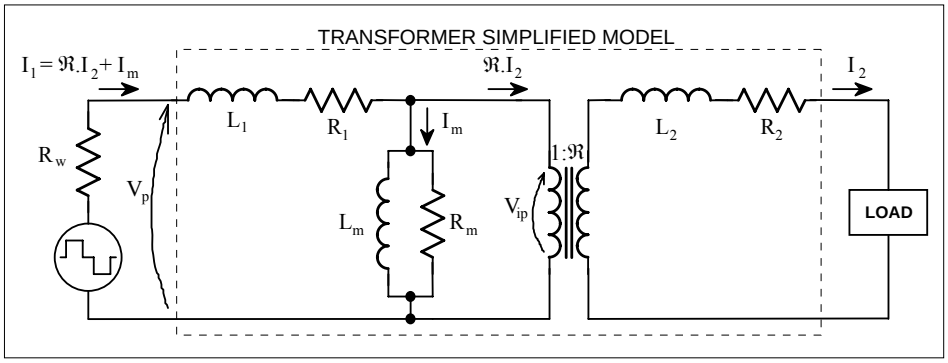


Figure 4.4 - Simplified transformer model.

To avoid transformer-unbalancing, internal voltage V_{ip} must not present DC level, otherwise the magnetizing current I_m will present a DC component (and also high peak values) and the transformer becomes saturated in one direction. The origin of DC level can be diverse, such as:

1) Asymmetry in the supply voltage V_p: in this case, V_{ip} is affected directly;
2) Half-wave load: in this case, voltage drops in the internal resistance of the voltage source and wires, as well as in the transformer impedances R_1 and L_1, occur in only one half-cycle, producing asymmetry in V_{ip};
3) Start-up conditions: at converter start-up or by suddenly inserting a load, V_{ip} can be submitted to a temporary voltage asymmetry. Although this condition is temporary, it can lead to high current peaks.

Figure 4.5 shows different situations that may occur.

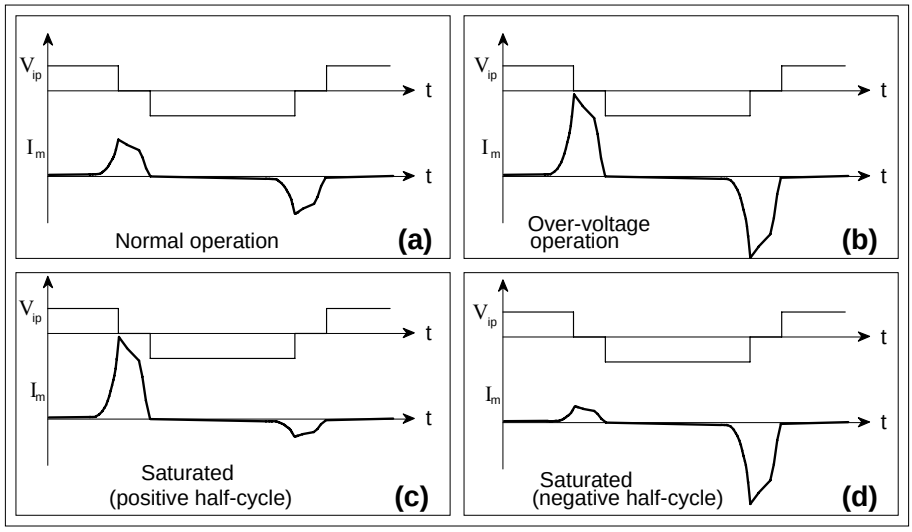


Figure 4.5 - Magnetizing current behavior under diverse conditions.

At normal operation condition, transformer magnetizing current is symmetric and presents relatively low peaks, as shown in figure 4.5(a). If the transformer is submitted

to an over-voltage (but still symmetric) condition, then the magnetizing current will be symmetric but will also present high peak values at the end of both half-cycles, as shown in figure 4.5(b). Normally, this situation is avoided by properly designing the transformer.

The situations shown in figures 4.5(c) and 4.5(d) can be caused by one of the cases mentioned previously. In these situations, unbalancing condition is immediately identified by the current asymmetry.

Despite of the problem origin, correction of unbalancing conditions involves two main tasks:

1) To identify the unbalancing condition;
2) To provide a mechanism to eliminate the primary voltage DC level.

Solutions for these both tasks are strongly dependent on the application.

4.4.2 *Identification of transformer-unbalancing*

Transformer unbalance condition can be identified by the detection of a DC level in the magnetizing current or in the voltage V_{ip} (internal point). For the former method, special attention must be given for the fact that practical measurements of the primary current may include load components. In this case, the circuit shown in figure 4.6 can be used to measure the magnetizing current even under the presence of load current.

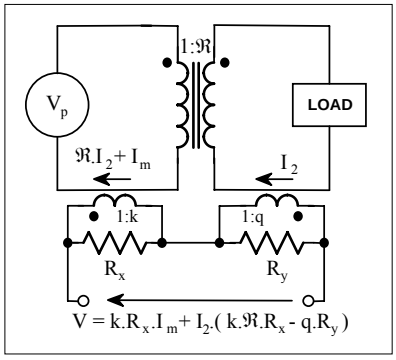


Figure 4.6 - Circuit to measure the transformer magnetizing current.

As can be seen in figure 4.6, through appropriate choice of the shunt resistances and relation-ratios of the current-transformers, it is possible to eliminate the secondary current I_2 from the given expression, thus obtaining a measurement voltage that is only proportional to I_m.

A measurement proportional to the internal primary voltage can be determined by using the circuit shown in figure 4.7.

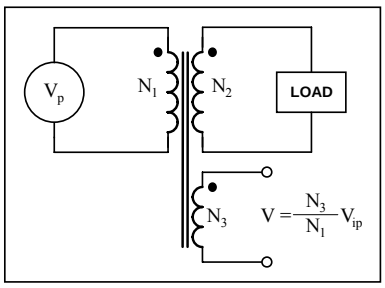


Figure 4.7 - Arrangement to measure the internal voltage of transformer primary.

In this case, an additional coil allows an accurate measurement proportional to the magnetizing flux derivative, which is also proportional to the internal primary voltage V_{ip}. This information can be used to detect an eminent unbalanced condition.

4.4.3 *The proposed method to identify unbalanced conditions*

Careful observation of figure 4.5 reveals that, in order to determine unbalanced conditions, it is not necessary to measure the magnetizing current along the entire cycle. In fact, unbalanced conditions can be identified by making measurements at the end of positive and negative intervals, as shown in figure 4.8.

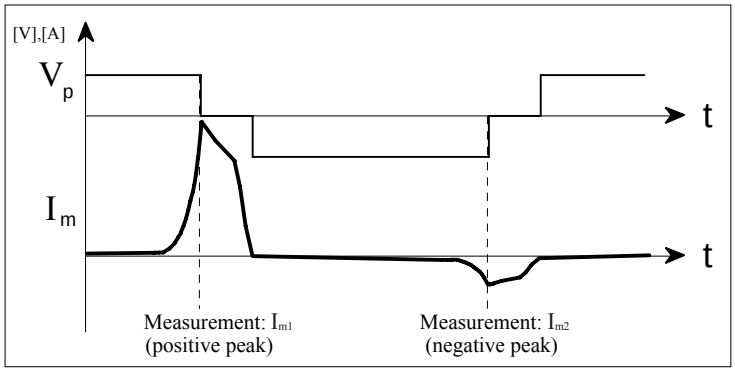


Figure 4.8 - Measurement instants to determine the unbalanced condition.

In this case, the positive peak I_{m1} is greater than the negative peak I_{m2}, revealing that the transformer is saturated in the positive direction.

Measurements of I_{m1} and I_{m2} can be done by taking advantage of a particular characteristic of the adopted topology: it allows to isolate transformer outputs from the load, making possible to do accurate measurements of the magnetizing current without influence of the load current. Figure 4.9 shows an example of how this process works.

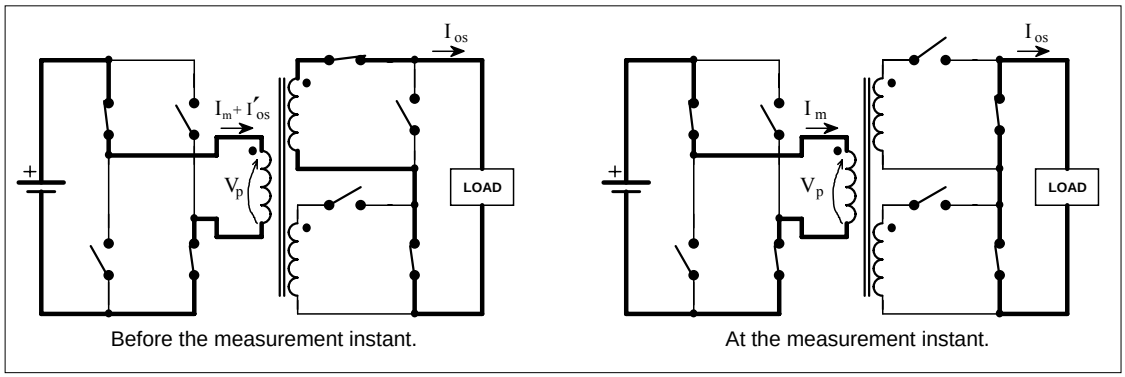


Figure 4.9 - Proposed process to measure the transformer magnetizing current.

As can be seen in figure 4.9, the transformer is disconnected from the load at the measurement instant, while another path for the load current is guarantied by the output-stage odd switches, what is particularly important in the case of inductive loads.

It also should be noted that the adopted measurement method does not disturbs the normal operation of the converter, since measurements happen near the end of each half-cycle, where the output voltage naturally should assume the zero value.

4.4.4 *The Proposed balance-control mechanism*

Once transformer-unbalancing condition has been detected, a control mechanism is used to compensate the problem by properly adjusting the H-bridge timing, as demonstrated in the example shown in Figure 4.10.

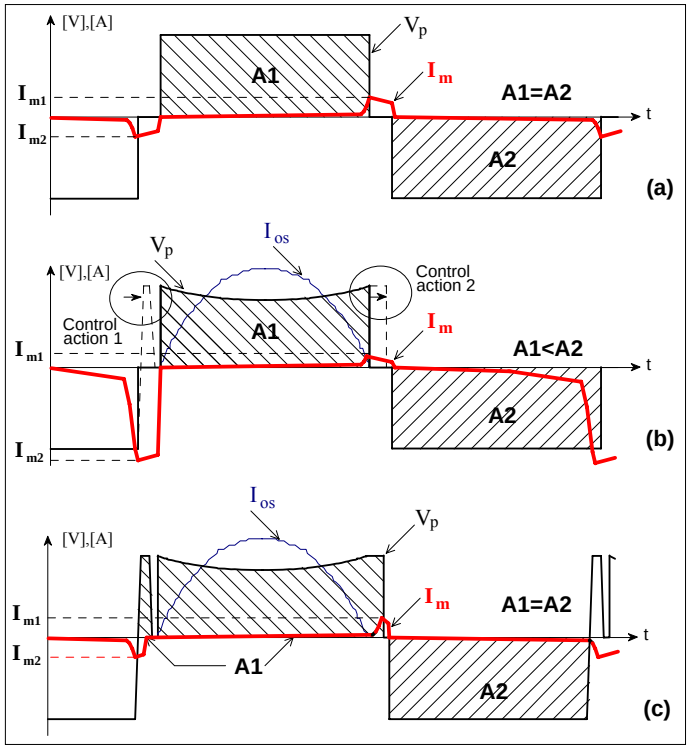


Figure 4.10 - Example of the proposed balance-control mechanism.

As can be seen in figure 4.10(a), under normal operation condition, the voltage produced by the H-bridge is perfectly balanced (no DC level) and the transformer magnetization current presents no indication of unbalancing[1].

On the other hand, if the converter feeds a half-wave load, as shown in Figure 4.10(b), then the voltage applied to the transformer presents a DC level due to voltage drops in the positive cycle. In consequence, the transformer becomes strongly saturated in the negative direction.

As also shown in figure 4.10(b), in a attempt to reestablish zero DC level in the transformer primary voltage, the proposed control mechanism provides a way to increase the positive cycle time period, so compensating its voltage drop. This control mechanism uses the hold-on-at-zero interval (T_z) in order to implement 2 actions:

Action 1: at the end of the negative voltage period, a floating time period replaces part of the hold-on-at-zero interval;

Action 2: the end of the positive voltage period is simply postponed, so replacing part of the hold-on-at-zero interval.

These two actions are simultaneously implemented and they are gradually increased until the magnetization current reaches again a symmetric condition ($I_{m1} = I_{m2}$), as shown in figure 4.10(c). Finally, it should be noted that the mechanism explained in this example can be applied for the unbalancing in the positive direction as well. In section 4.4.5, it is explained in detail how the action 1 of the balance-control mechanism works.

[1] In practice, it was observed that the transformer may present an asymmetric magnetizing current even if it is supplied with a zero dc level voltage. In other words, the balanced transformer operation can be only ensured by using closed loop control, such as the one described in this work.

4.4.5 *Detailed analysis of the balance-control action 1*

The control action 1 corresponds to a time period when all H-bridge switches are held on the off state and consequently no fixed[1] voltage is imposed to the transformer primary. It is introduced in the hold-on-at-zero interval that precedes the half-cycle under correction.

Without loss of generality, it is considered, for explanation purpose, a typical correction of the positive half-cycle. For this case, the time diagram and the operation intervals are shown in figures 4.11 and 4.12, respectively.

As can be seen in figure 4.11, the control action 1 is divided in 3 operation intervals (II, III and IV), which replaces part of the hold-on-at-zero interval. The descriptions of each interval follow:

Interval I: it is part of the negative period. Before its end, the output-stage is disconnected from the load and after that only the magnetizing current flows through the transformer primary. At the end of this interval, the magnetization current reaches its maximum value.

Interval II: it begins when all H-bridge switches are driven to the off state, so initiating also the control action 1. The magnetization current flows through the switch snubbers and the voltage applied to the transformer primary rises with a rate defined by the snubbers capacitors and also by the magnetization current intensity. It ends when the magnetization currents starts to flow through the reverse diodes of the H-bridge switches.

Interval III: at this interval the voltage applied to the transformer primary is clamped to a positive value slightly higher (due to the reverse diodes voltage drops) than the input DC voltage V_b.

Interval IV: it is the last interval of the control action 1, which begins when the magnetization current changes its sign. The magnetization current flows through the switch snubbers and its falling rate is defined by the snubber capacitors and transformer magnetization inductance. It ends when the transformer primary voltage is forced to be zero.

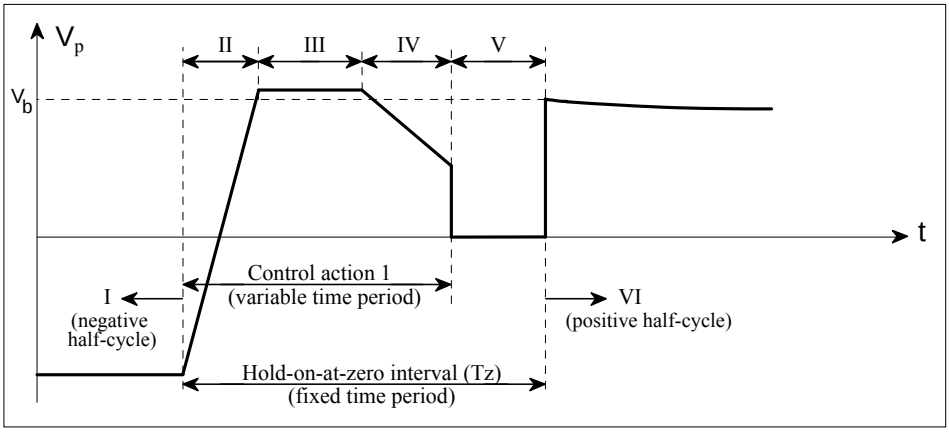


Figure 4.11 - Detailed time diagram for the control action 1 (typical case).

[1] This is the origin of the term "floating".

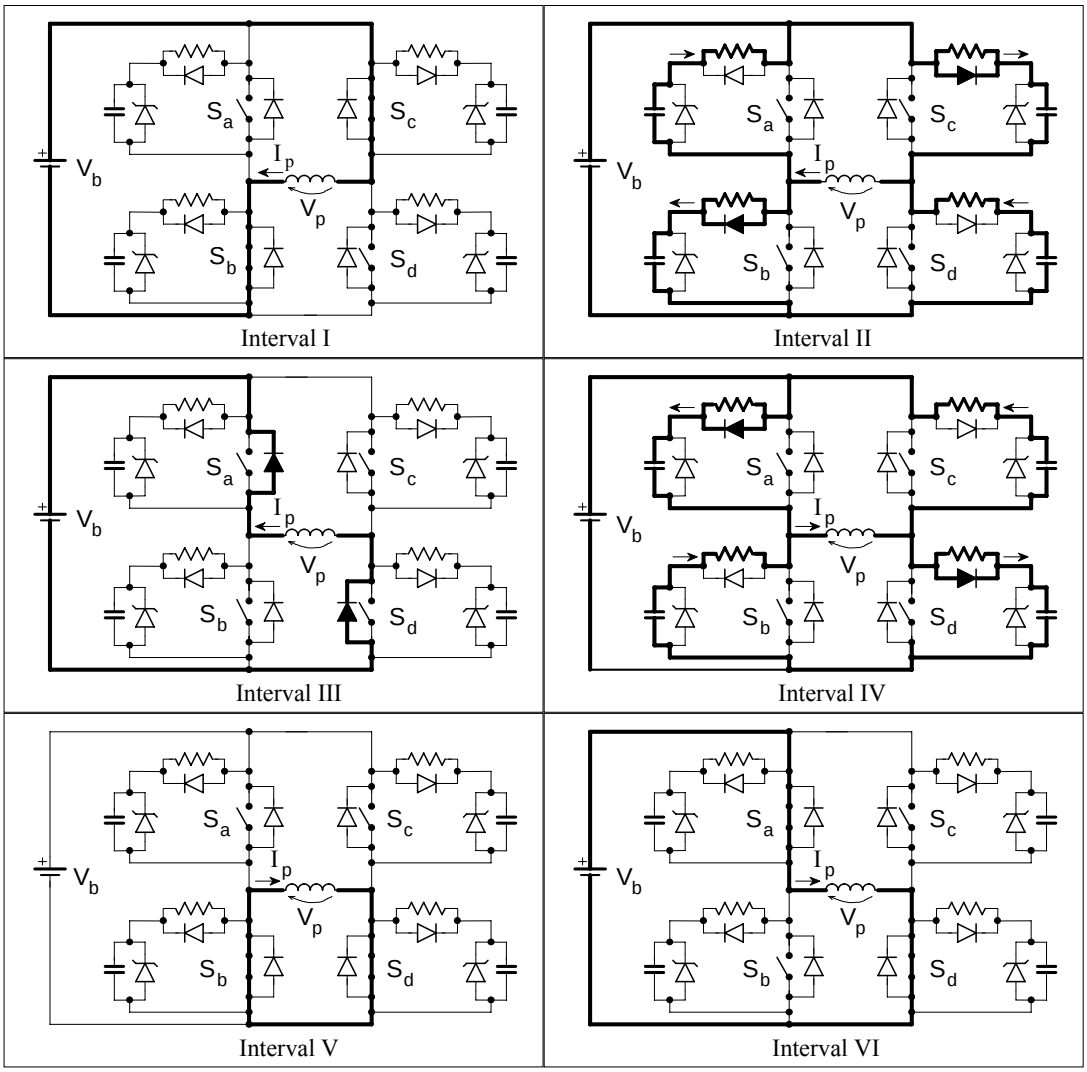


Figure 4.12 - Operation intervals of the control action 1.

Interval V: this is the remaining time of the hold-on-at-zero interval that was not replaced by the control action 1. During this interval, the transformer primary coil is short-circuited by the H-bridge switches S_b and S_d. It ends when the positive cycle starts.

Interval VI: it is simply the start of the positive cycle.

As explained, it is possible to conclude that the control action 1 contribution to the V_p DC level reduction is not fixed. In fact, its contribution is influenced by the magnetization current in a way that fine balance is automatically generated by the hardware. In other words, if the magnetization current increases then the intervals II and IV will be shorter, while interval III will be longer, increasing the correction action. On the other hand, if the magnetization current is reduced excessively (what can indicate that the unbalancing condition has been inverted) then interval II will be extended, decreasing or even inverting the control action 1 correction.

Finally, it should be noted that the smoothness of the described self-balance-control is dictated by the amplitude of the voltage V_p applied to the transformer. Figure 4.13 shows what can happen if the voltage V_p is too high or too low. As shown in figure 4.13(a), if the transformer is under an over-voltage condition, the magnetization current presents high peaks and the intervals II and IV can practically disappear. As a result, the

control action 1 lost its capacity of fine self-balance. In this case, its correction is practically fixed, like the control action 2.

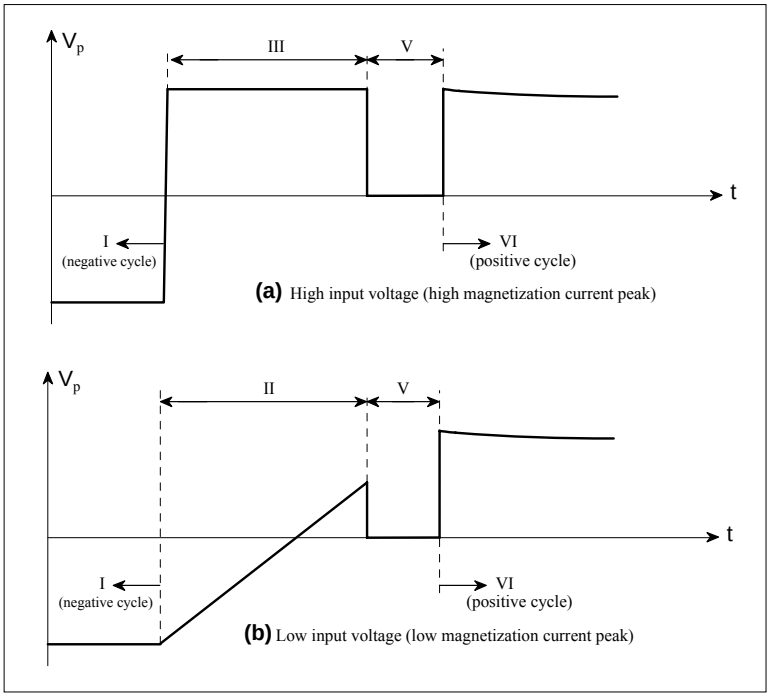


Figure 4.13 - Time diagram for the control action 1 (under extreme conditions).

On the other way, if the transformer is fed by a low voltage, its magnetization current is small and the fine self-balance became very smooth, as can be seen in figure 4.13(b). In this case, the operation intervals III and IV may even do not exist.

4.4.6 *Limitation of the proposed balance-control mechanism*

The capability of the proposed method to correct the presence of a DC level in the transformer primary voltage and avoid an unbalancing condition is limited by the extensions of the control actions. In practice, the control actions extensions are limited by the hold-on-at-zero interval width, and the latter is limited by the allowed amount of distortion it can introduce in the inverter output waveform. In fact, compromise exists between the correction range and the allowed output voltage distortion.

It is important to note that the equivalent series resistance of the DC source affects directly the performance of the proposed method (in terms of the maximum allowed amount of unbalanced load that can be supported).

4.4.7 Correction of the output voltage DC level

Correction of the output voltage DC level was not investigated in this work. In fact, the proposed balance-control only avoids transformer-unbalancing within the inverter, and any DC level correction is applied to the output voltage. This can be a problem to the operation of a half-wave load in conjunction with an inductive load.

One possible solution to this problem is to control the DC level by modifying the up part of the multilevel waveform.

4.5 Waveform optimization

4.5.1 *Straightforward waveform formation*

Straightforward approximation of a sinus by a multilevel waveform is demonstrated in figure 4.14, which shows the case of a waveform with p = 3.

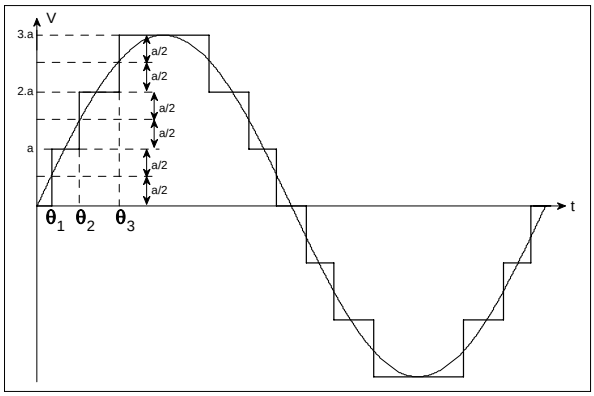


Figure 4.14 - Straightforward formation of a multilevel waveform.

This approximation can be easily extended to any number of levels and it is evident that better concordance is achieved as the number of levels is increased. In terms of numbers, table 4.3 shows the THD and M_i for waveforms with diverse values of p.

Table 4.3 - THD and M_i for diverse p values (straight forward formation).

p	5	6	7	8	9	10	11	12	13	15	20	25	30	31
THD_{13}	2.51	1.83	1.32	0.97	0.74	0.59	0.48	0.41	0.36	0.29	0.20	0.16	0.13	0.12
THD_{40}	6.28	5.10	3.81	2.73	2.30	1.95	1.70	1.49	1.35	1.02	0.65	0.40	0.28	0.27
THD_{50}	6.36	5.29	4. 50	3.89	2.84	2.39	2.07	1.64	1.46	1.17	0.78	0.51	0.40	0.38
THD_{63}	6.78	5.49	4.61	3.98	3.54	3.16	2.51	2.11	1.78	1.46	0.84	0.62	0.47	0.45
M_i	1.013	1.009	1.007	1.006	1.005	1.004	1.004	1.003	1.003	1.002	1.001	1.001	1.001	1.001

THD_{xy} : up to xy^{th} harmonic.

Just for comparison purpose, table 4.3 shows the THD calculated up to the 13^{th}, 40^{th}, 50^{th} and 63^{rd} harmonic. This work adopts THD_{50} as default.

4.5.2 *Multilevel waveform voltage regulation*

Two different methods can be used to control the RMS value of a multilevel waveform: changing number of levels or changing waveform shape. Figure 4.15 illustrates how these methods work.

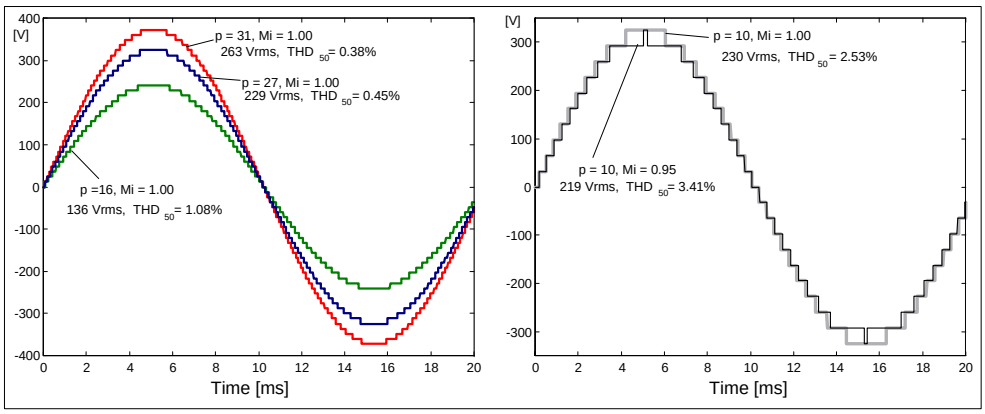


Figure 4.15 - Methods to implement voltage regulation in a multilevel waveform.

An ideal control strategy should combine these to methods in order to provide good voltage regulation while keeping M_i close to 1.00 and THD as low as possible. Table 4.4 shows how THD is affected by M_i changes.

Table 4.4 - THD for diverse p and M_i (improved waveforms).

p	5	6	7	8	9	10	11	12	13	15	20	25	30	31
M_i = 0.970	7.60	6.20	5.29	4.56	3.54	3.00	2.62	2.38	2.08	1.68	1.07	0.47	-	-
M_i = 0.980	7.32	5.93	5.06	4.34	3.34	2.74	2.44	2.23	2.02	1.64	1.03	0.75	0.50	0.46
M_i = 0.990	6.91	5.67	4.85	4.12	3.00	2.55	2.25	2.01	1.71	1.37	0.93	0.73	0.59	0.57
M_i = 1.000	6.62	5.45	4.65	3.95	2.90	2.45	2.12	1.66	1.49	1.14	0.79	0.55	0.44	0.41
M_i = 1.010	6.40	5.27	4.47	3.76	2.79	2.31	1.92	1.56	1.32	1.09	0.68	0.50	0.41	0.40
M_i = 1.020	6.21	5.13	4.37	3.41	2.72	2.25	1.75	1.59	1.44	1.25	0.94	-	-	-
M_i = 1.030	6.11	5.09	4.32	3.39	2.76	2.26	2.00	1.87	1.76	1.57	1.87	-	-	-

THD : up to 50th harmonic.

The results shown in table 4.4 are not so straightforward achieved as those presented in table 4.3, but they are improved waveforms (minimum THD criteria) that were determined by dedicated software. This software was specially developed to this work and it is a powerful tool capable to generate, analyze and improve high-resolution multilevel waveforms (short-guide manual is found in Appendix B).

4.5.3 W*aveforms with hold-on-at-zero interval*

As discussed in section 4.4, the adopted balance-control method introduces in the inverter output voltage relatively long periods at the zero level (T_z). In consequence, THD is increased and the introduced distortion near zero crossing is clearly perceptible, as shown in figure 4.16.

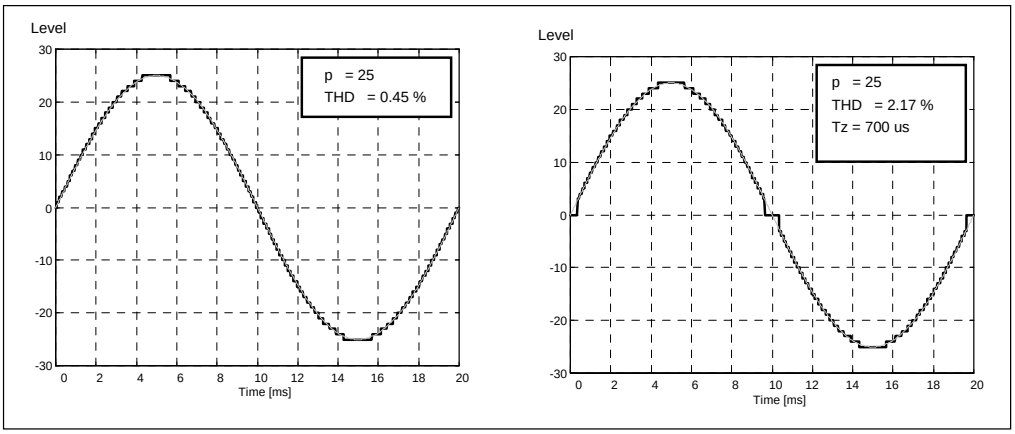


Figure 4.16 - Multilevel waveforms with and without hold-on-at-zero interval.

In fact, the amount of THD increase depends on T_z and p values, as shown in table 4.5. As can be seen, the hold-on-at-zero interval may be the dominant distortion factor for waveforms with large p.

Table 4.5 - THD for diverse p and T_z (not smoothed, improved).

p	5	6	7	8	9	10	11	12	13	15	20	25	30	31
Not defined	6.09	5.07	4.43	3.55	2.78	2.35	1.85	1.53	1.17	1.09	0.67	0.45	0.31	0.30
T_z= 400 µs	6.09	5.07	4.43	3.57	2.78	2.44	2.05	1.72	1.59	1.44	1.10	0.97	0.93	0.93
T_z= 500 µs	6.09	5.07	4.39	3.62	2.98	2.65	2.31	2.03	1.88	1.71	1.41	1.38	1.30	1.29
T_z= 600 µs	6.09	5.07	4.37	3.86	3.32	2.84	2.49	2.26	2.17	1.96	1.84	1.73	1.71	1.72
T_z= 700 µs	6.14	5.13	4.56	4.16	3.70	3.04	2.74	2.62	2.44	2.35	2.27	2.17	2.15	2.13
T_z= 800 µs	6.30	5.33	4.93	4.52	4.12	3.25	3.03	3.01	2.91	2.91	2.71	2.71	2.70	2.70

THD: up to 50th harmonic.

In practice, in addition to THD and M_i parameters, the voltage versus time characteristic of a multilevel waveform must be careful analyzed. Taking this into account, special attention must be given to the large voltage steps generated in consequence of the forced hold-on-at-zero interval. This problem can be minimized by adding some "smoothness" at the hold-on-at-zero interval borders, as illustrated in figure 4.17.

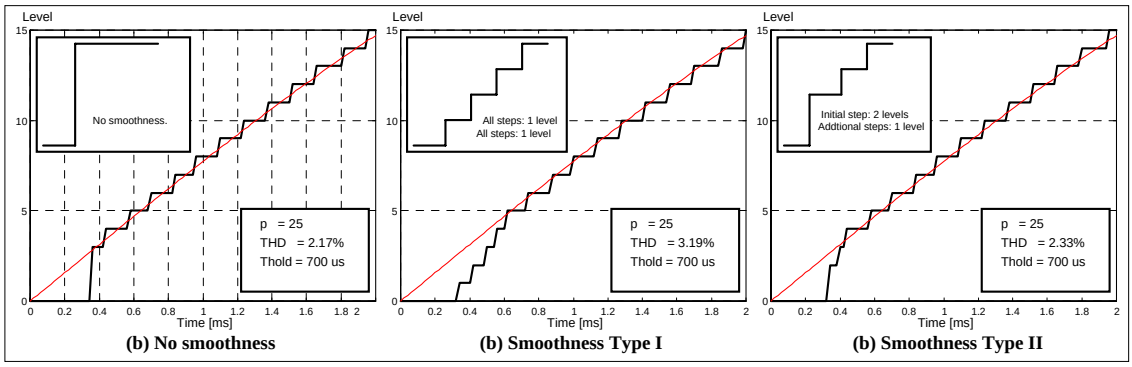


Figure 4.17 - Examples of waveform smoothness.

As can be seen, THD increases when the waveform is smoothed and higher smoothness (type I) implicates in higher THD. It also should be noted that the smoothness waveforms showed in figure 4.17 uses a time interval of 75 μs between each additional step (results may vary according to this interval width). Table 4.6 shows the effect of the proposed smoothness methods on the THD for diverse values of p. Shadowed values show a possible practical choice of smoothness type.

Table 4.6 - THD for diverse p and smoothness (T_z = 700 μs, interval = 75 μs, improved).

	Number of levels per quarter cycle (p)													
Smooth.	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**15**	**20**	**25**	**30**	**31**
Without	6.14	5.13	4.56	4.16	3.70	3.04	2.74	2.62	2.44	2.35	2.27	2.17	2.15	2.13
Type I	6.14	5.13	4.56	4.16	3.70	3.04	2.74	2.62	2.44	2.53	2.87	3.16	3.69	3.83
Type II	-	-	-	-	-	-	-	-	-	2.35	2.27	2.46	2.75	2.83

THD: up to 50th harmonic.

4.5.4 *Effect of the controller resolution*

Practical implementation using digital circuits may appreciably modify the theoretical multilevel waveform timing, as shown in figure 4.18.

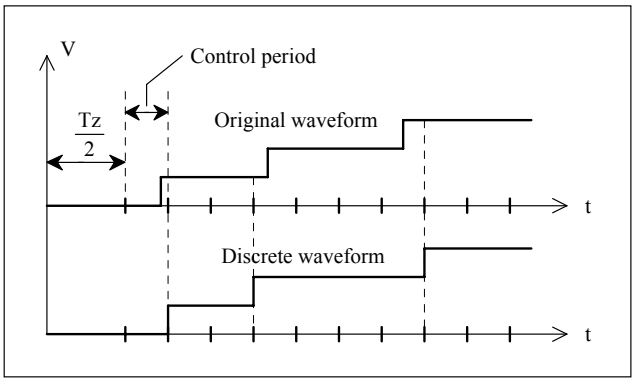


Figure 4.18 - Effect of controller resolution in the theoretical waveform.

In fact, the digital controller used in this work is based on a control period (T_c) of 75 μs, which means that each step transition occurs only in time instants that are multiple of 75 μs.

4.5.5 *Final waveforms data*

Final design of the implemented multilevel waveforms included:

- Waveform improvement (lowest THD_{50} criteria);
- 700 μs hold-on-at-zero interval;
- Smoothness of the hold-on-at-zero interval borders;
- 75 μs control interval.

Basic information data (THD_{50}, Mi and initial step) for the final waveforms are presented in table 4.7. As can be seen, the calculated THD_{50} is under 3 %, M_i is close to 1.00 and maximum step height is equal to 2 levels.

Programming code for the final waveforms is listed in Appendix C.

Table 4.7 - THD, Mi and maximum step for the final waveforms.

p	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
THD_{50}	2.80	2.90	2.83	2.91	2.96	3.02	3.04	3.14	2.50	2.58	2.63	2.68	2.71	2.75	2.82	2.85
M_i	1.004	0.999	1.000	1.000	0.999	0.996	0.995	0.997	0.997	0.998	0.997	0.996	0.997	0.998	0.999	0.998
Init. Step	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2

THD : up to 50th harmonic.

4.5.6 *Firmware update*

At the final implementation, the controller firmware was modified to support the transformer-unbalancing control feature, but the lookup tables were not updated. In consequence, the implemented waveforms do not correspond exactly to the waveforms described in section 4.5.5.

Fixed lookup tables (in accordance with the operation of the new firmware) are the ones listed in appendix C. The controller firmware, presented in appendix D, is the implemented version (as it is, without any modification) and it is not fixed.

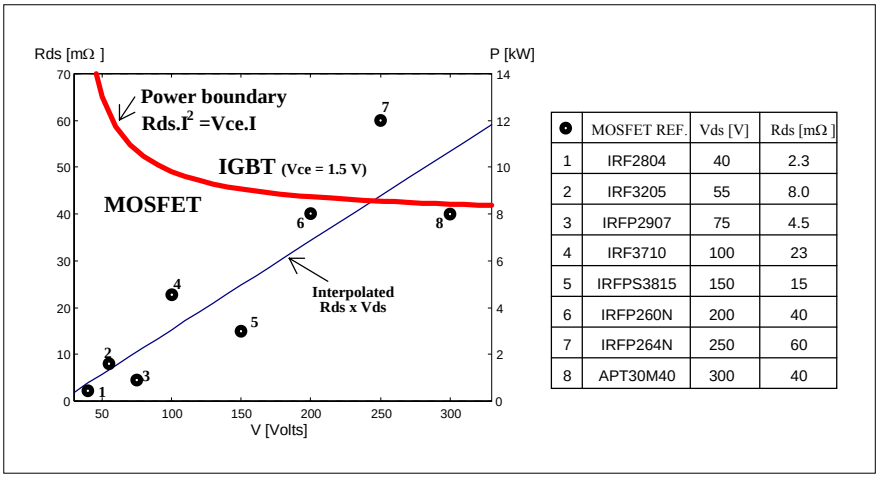
It is recommended that future work should modify the controller firmware to use the correct lookup tables given in appendix C.

4.6 Bi-directional switch configuration

4.6.1 *Selection of the switches technology*

Nowadays, there are two widespread and cost-effective technologies suitable for the implementation of the proposed converter switches: MOSFETs and IGBTs. Because both technologies are available for the intended operation voltage, current and frequency, selection of the most appropriated technology is done based on the efficiency criteria.

In the proposed inverter, switching frequency is in the range from line frequency to few kHz and switching losses can be neglected. Considering that an IGBT in conduction state may be modeled by a constant 1,5 V voltage drop (V_{ce}) and a MOSFET by a constant resistance (R_{ds}) then it is possible to define an usage boundary, as shown in figure 4.19.



	MOSFET REF.	Vds [V]	Rds [mΩ]
1	IRF2804	40	2.3
2	IRF3205	55	8.0
3	IRFP2907	75	4.5
4	IRF3710	100	23
5	IRFPS3815	150	15
6	IRFP260N	200	40
7	IRFP264N	250	60
8	APT30M40	300	40

Figure 4.19 - Power boundary to define best usage of MOSFETs and IGBTs.

From figure 4.19, it is possible to conclude that MOSFETs are the best choice to implement all switches in this work, since working voltage of any switch is under 300 V and the inverter power is in the range of few kW.

4.6.2 *Selection of the bi-directional configuration*

According to section 4.1, all output-stage switches must be capable to operate with AC voltage and current. In practice, this type of switch is not yet available as a single component. However, using MOSFETs, it can be implemented by association of some components, as shown in figure 4.20.

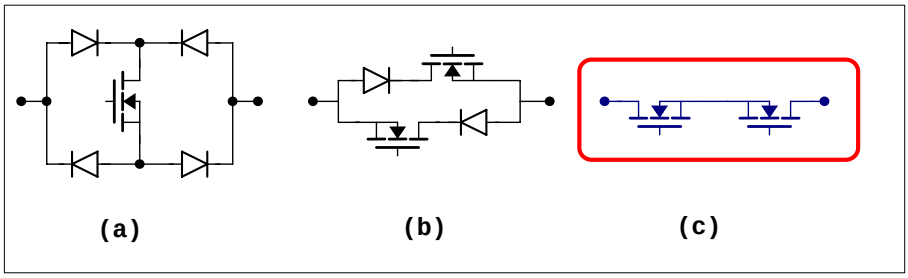


Figure 4.20 - Different bi-directional switch implementation using MOSFETs.

Configuration (c) was chosen because it can provide lower losses when compared to (a) and (b), due to the low resistance of modern MOSFETS and also due its bi-directional channel conduction capability. In this case, when both MOSFETs of configuration (c) are on, it can be modeled as a resistance of 2 times the value of R_{ds} of a single MOSFET.

4.6.3 *Ideal switch control*

In the operation description found in section 4.1, it was assumed that the output-stage switches were ideal and also there was not considered any time delay between switches of a same output-stage element.

In practice, MOSFETs have non-zero switching-time, and dead-times must be included in the switch signals in order to avoid short-circuits. In consequence, the introduced dead-times can be critical when the converter feeds inductive loads, which requires always a path for its current to circulate. This problem can be solved by individually controlling each switch, according to the load current direction and transformer voltage polarity, resulting in four distinct signals sequences.

Figures 4.21 and 4.22 illustrate two situations, considering the same output voltage polarity but different load current directions.

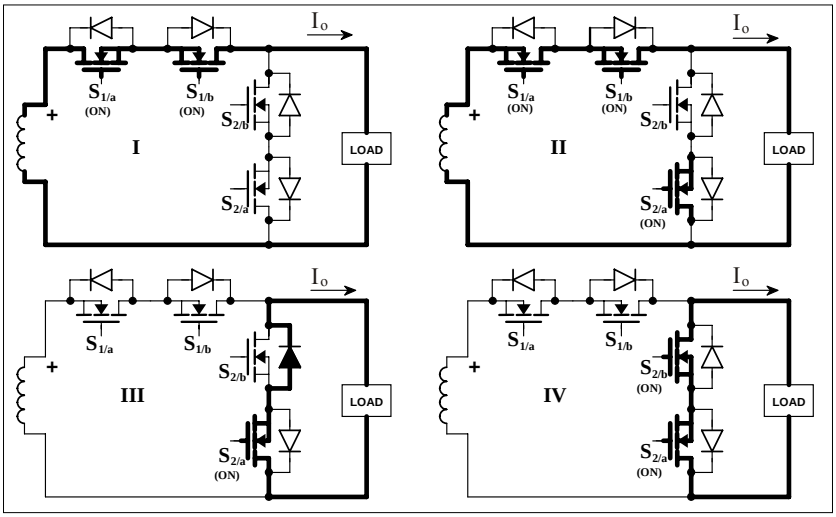


Figure 4.21 - Ideal switch control (Case I: normal current flow).

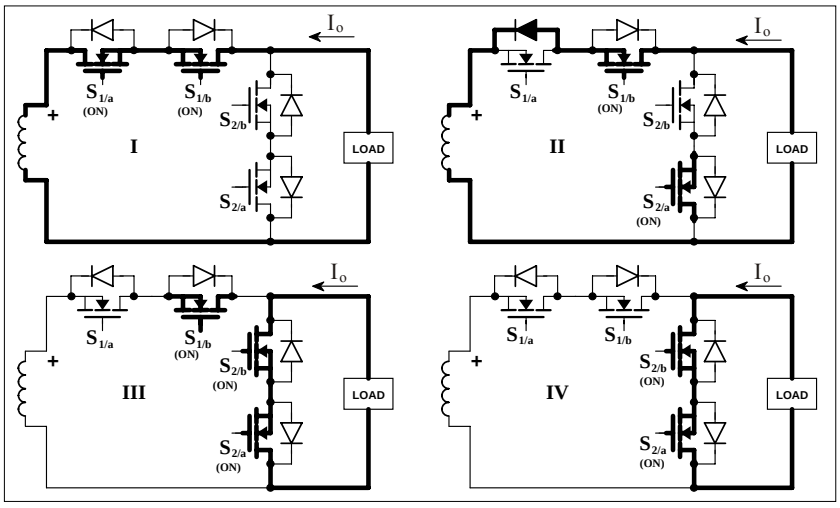


Figure 4.22 - Ideal switch control (Case II: reverse current flow).

4.6.4 *Implemented switch control*

In practice, to achieve lower no-load consumption and to decrease costs, both switches are driven at the same time and by the same drive. In this case, when the inverter feeds an inductive load, the switch snubbers must provide a path for the load current during the dead-time interval (approximately 2 μs).

Figure 4.23 shows an example of an output-stage transition under inductive load current.

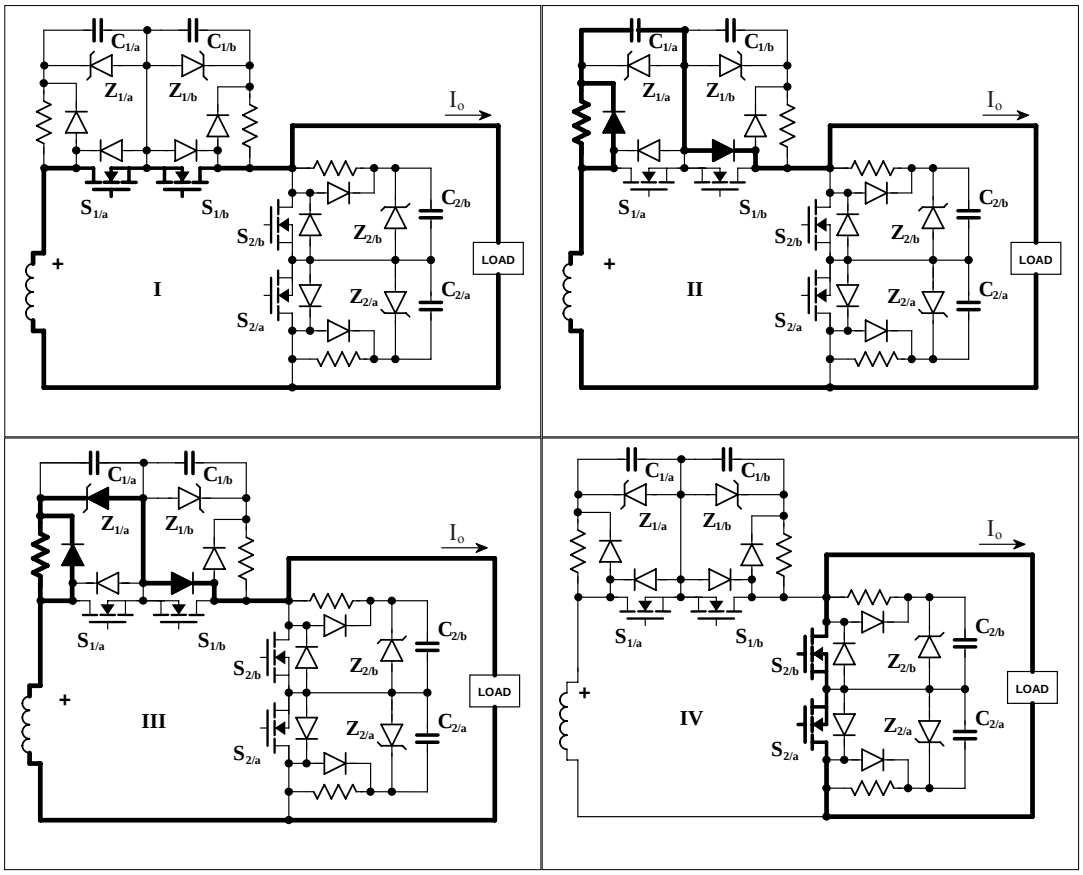


Figure 4.23 - Implemented output-stage switch control.

As can be seen in figure 4.23, the introduced dead-time correspond to a time period where all switches are off (intervals II and III) and the load current is forced to circulate through the snubber/clamp circuit and MOSFET's body diode. During interval II, the load current charges the snubber capacitor, limiting the dv/dt rate applied to the switch $S_{1/a}$. During interval III, the current flows though the clamp zenner diode and the voltage applied to the switch $S_{1/a}$ is clamped to a safe value.

It should be noted that, under certain circumstances (depending on the rated voltage of the zenner and MOSFET), the zenner clamping voltage can exceed the breakdown voltage of the MOSFET and the current may be shared between the zenner diode and the MOSFET. In this case, the MOSFET operates in a controlled avalanche mode. However, because the time duration and the energy is relatively small, it is not expected that such condition can cause deterioration of the zenner or MOSFET.

In conclusion, the snubber/clamp circuit does not only absorb spurious energy peaks but it carries the total output current in some cases, making it indispensable. Because switching frequency is relatively low and dead-times are very short, no appreciable power is dissipated due to this process.

4.7 Prototype design

In order to compare the prototype with some existing commercial inverters, special care was taken while designing the prototype. As a result, the experimental set-up was not designed to work only in a laboratory environment, but it is a full-functional inverter (unclosed version).

4.7.1 *Design specifications*

The adopted design specifications are listed in table 4.8.

Table 4.8 - Design specifications.

Rated power	3000 kVA
Rated input voltage	48 V
Output voltage	230 V_{CA} / 50 Hz
Voltage regulation	+5 % , -10 %
THD	< 5 %,

Although these specifications were arbitrary defined, they are based on the following facts:

- A 3 kVA inverter fits to several SARES applications and it is a reasonable value to validate the proposed topology. Also, several commercial inverters are rated to 3 kVA, and posterior comparison between the proposed inverter and similar products can be done;
- An input voltage of 48 V is suitable for a 3 kVA power rating (regarding current level) and it does not present major isolation safety concerns. In addition, it can be considered a standard value commonly used in SARES applications;
- Output voltage of 230 V_{AC} / 50 Hz is the standard utility voltage in Germany, where the inverter will be implemented and tested;
- Adopted values of voltage regulation and THD attend current utility standard limits [92,93].

4.7.2 *Multilevel waveform resolution*

Design of the multilevel waveform resolution depends on many factors, such as DC input voltage range, AC output voltage range, internal voltage drops and allowed THD contents. Thus, while a precise mathematical model is relatively complex to build, good design can be done by using table 4.9.

Table 4.9 - Approximated minimum voltage regulation as a function of p (THD < 5 %).

p	7	8	9	10	11	12	13	15	20	25	30
Regulation (M_i=1.00) [%]	7.1	6.3	5.6	5.0	4.5	4.2	3.8	3.3	2.5	2.0	1.7
Regulation (M_i not fixed) [%]	5.5	< 1	< 1	< 1	< 1	< 1	< 1	< 1	< 1	< 1	< 1

THD : up to 50th harmonic.

The first line of table 4.9 corresponds to the minimum voltage regulation that can be achieved for M_i=1. If it is allowed to regulate the amplitude with the disadvantage of worst crest factor (limited to THD < 5 %), then it is possible to achieve regulation of less than 1 % for any p > 7, as showed in the second line of table 4.9.

For example, if voltage compensation of about 40 % is needed to compensate all mentioned factors (while THD < 5 % and voltage regulation within $\pm$ 5 %), then minimum number of levels that must be used is 12. In this case, RMS voltage control is

provided by changing the number of output levels from 8 to 12 and also by adjusting the value of M_i.

In this work, it was adopted p = 31 (5 cells) and voltage control was done solely by changing the number of output levels from 15 to 31 (M_i always approximately equal to 1, what implies in better waveform quality). Thus, the input voltage can be reduced/increased more than 50% while maximum voltage deviation is within {-10 %, +5 %}, as desired.

4.7.3 *Transformer specification*

The implemented prototype made use of a multi-winding-transformer already available. Table 4.10 shows the transformer data.

Table 4.10 - Transformer data.

Rated power	3000 VA
Primary coil	48 V - 6,8 mΩ
Secondary coil 1	12 V / 8,06 A - 18 mΩ
Secondary coil 1	24 V / 8,06 A - 27 mΩ
Secondary coil 1	48 V / 8,06 A - 44 mΩ
Secondary coil 1	96 V / 8,06 A - 75 mΩ
Secondary coil 1	192 V / 8,06 A - 130 mΩ
No-load losses @48 V (RMS - square)	13 W
Weight	32 Kg
Size	290x108 mm
Core	Toroidal
Conformity	EN 61558

Power, voltages and currents: from manufacturer. Resistances: measured values.

Although this transformer have been used to implement the prototype, precise transformer design must take into account that actual currents are higher than that specified by a standard transformer design, as the case of the available transformer.

In fact, transformer primary current can be calculated from equation 4.8, and secondary coils must be capable to carry approximately the nominal load current.

4.7.4 *Specification of switches and snubbers*

Considering an approximation of the nominal operation point (η = 90 %, 3000 kVA @ V_b = 48 V, V_o = 230 V), the input and output currents are approximately 85 A_{RMS} and 13 A_{RMS}, respectively. It was also considered that the switches rated current should be around four times more (340 A_{RMS} and 52 A_{RMS}), so the prototype can support surge power and also temperature rise. Table 4.11 shows the switches and snubbers specifications used in the implemented prototype [94,95].

Table 4.11 - Component data for all partial output-stage modules.

Stage	[V]	MOSFET DATA				Z_n [V]	R_n [Ω]	C_n [nF]
		Reference	V_{ds} [V]	I_d [A]	R_{ds} [mΩ]			
H-bridge	48	2x IRFP2907	75	2x 209	4,5 / 2	66	330	470
Out. Stage 1	12	IRF3205	55	110	8	22	120	47
Out. Stage 2	24	IRF3205	55	110	8	34	330	47
Out. Stage 3	48	IRF2807	75	82	13	66	330	47
Out. Stage 4	96	IRFP260N	200	50	40	130	470	47
Out. Stage 5	192	APT30M40LVR	300	76	40	250	470	47

It is important to note that MOSFET selection also took into account availability, price and conduction resistance. For example, the IRF3205 could be replaced by either IRF48N (55 V, 64 A, 14 mΩ) or by the IRF2805 (55 V, 175 A, 4.7 mΩ). The IRF3205 was selected due to its intermediate value of cost/performance ratio. On the other hand, the IRFPS3815 (150 V, 105 A, 15 mΩ), could replace the low performance IRFP260N, but it was not available.

Finally, it is interesting to observe how the MOSFETs conduction losses are distributed along the diverse inverter stages, as shown in figure 4.24. As can be seen, conduction losses due to the 12 V output-cell correspond to only 4 % of the total switches conduction losses and it decreases total converter efficiency in about 0.15 %.

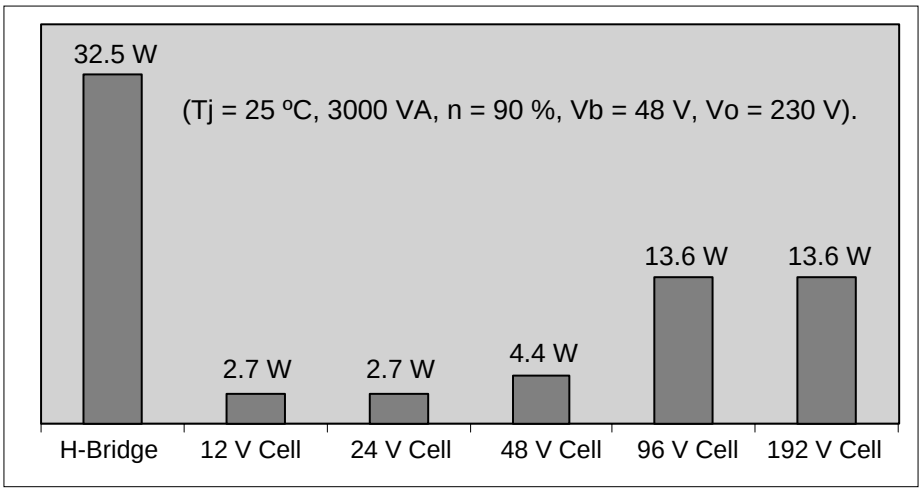


Figure 4.24 - Estimated switch losses per output-cell.

4.8 Simulation

Simulation of the investigated inverter presented some difficulties due to the required large number of digital control signals. As a matter of fact, use of the improved waveforms, discussed in section 4.5, did not make practical to generate control signals by means of standard analog/digital circuits and a special computer program, shortly discussed in section 4.8.1, had to be developed.

All simulations were restricted to specific static operation points.

4.8.1 *Simulation tool*

Simulations were done using OrCAD 9.1 toolbox, which is based on PSPICE simulation program. Although OrCAD can be considered one of the most powerful simulation software currently available, it was noted that it does not include an adequate tool to generate sets of complex digital signals, such those required by a high resolution multilevel inverter.

In fact, operation of the proposed inverter requires 14 digital signals and a total of about 450 transition or 900 time instant definitions (p = 31). This means that any change in the waveform shape, rise/fall times or dead-time implies in change 900 lines within 14 text files.

Such hard work motivated the development of a pseudo-language capable to describe several drive signals in a compact and flexible format. A compiler was also developed (using C language) to process this pseudo-code, generating several output text files (signal files). Figure 4.25 shows an example of pseudo-code (p = 31), signal file and compiler screen.

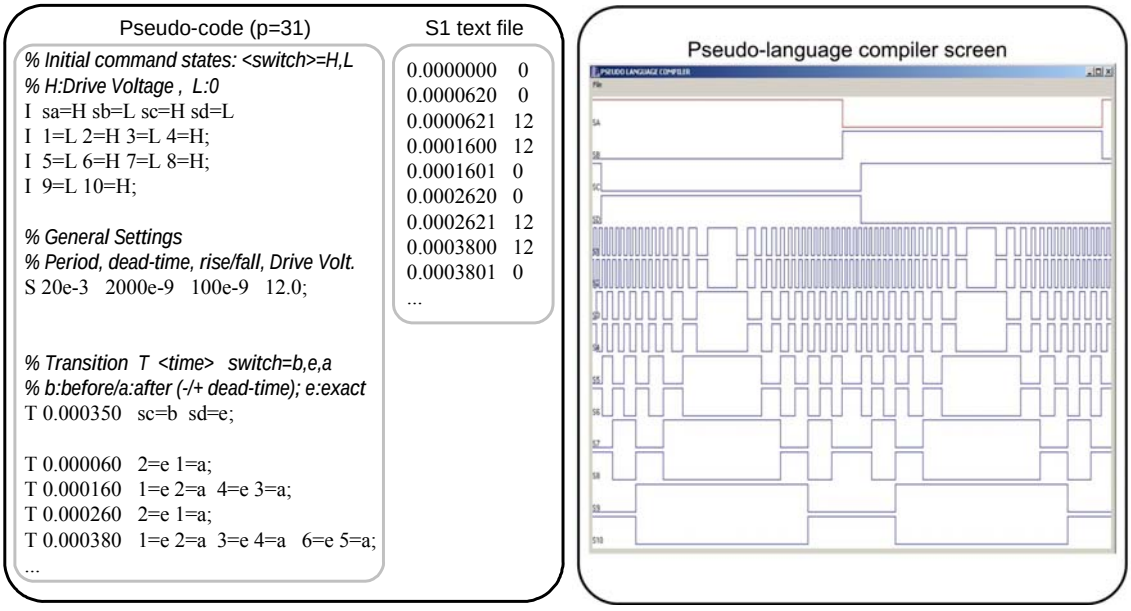


Figure 4.25 - Example of pseudo-code, signal text file and compiler screen.

As can be seen, the pseudo-code is simple and the example of generated signal file includes the specified dead-time and rise/fall times. The compiler also includes a graphic interface, where all defined signals are displayed. A complete pseudo-language code (p = 27) is found in appendix E.

4.8.2 *Simulation of the initial structure*

According to the prototype design presented in section 4.7, the main structure of a 5-stage inverter was defined and its correspondent simulation schematic circuit is shown in figure 4.26. As can be seen, 14 signals files are used in the simulation, which were generated by the developed tool described in section 4.8.1.

The value of p was adopted as 27 in all simulations, providing an output voltage of about 230 V_{CA} for the nominal input voltage of 48 V_{DC}.

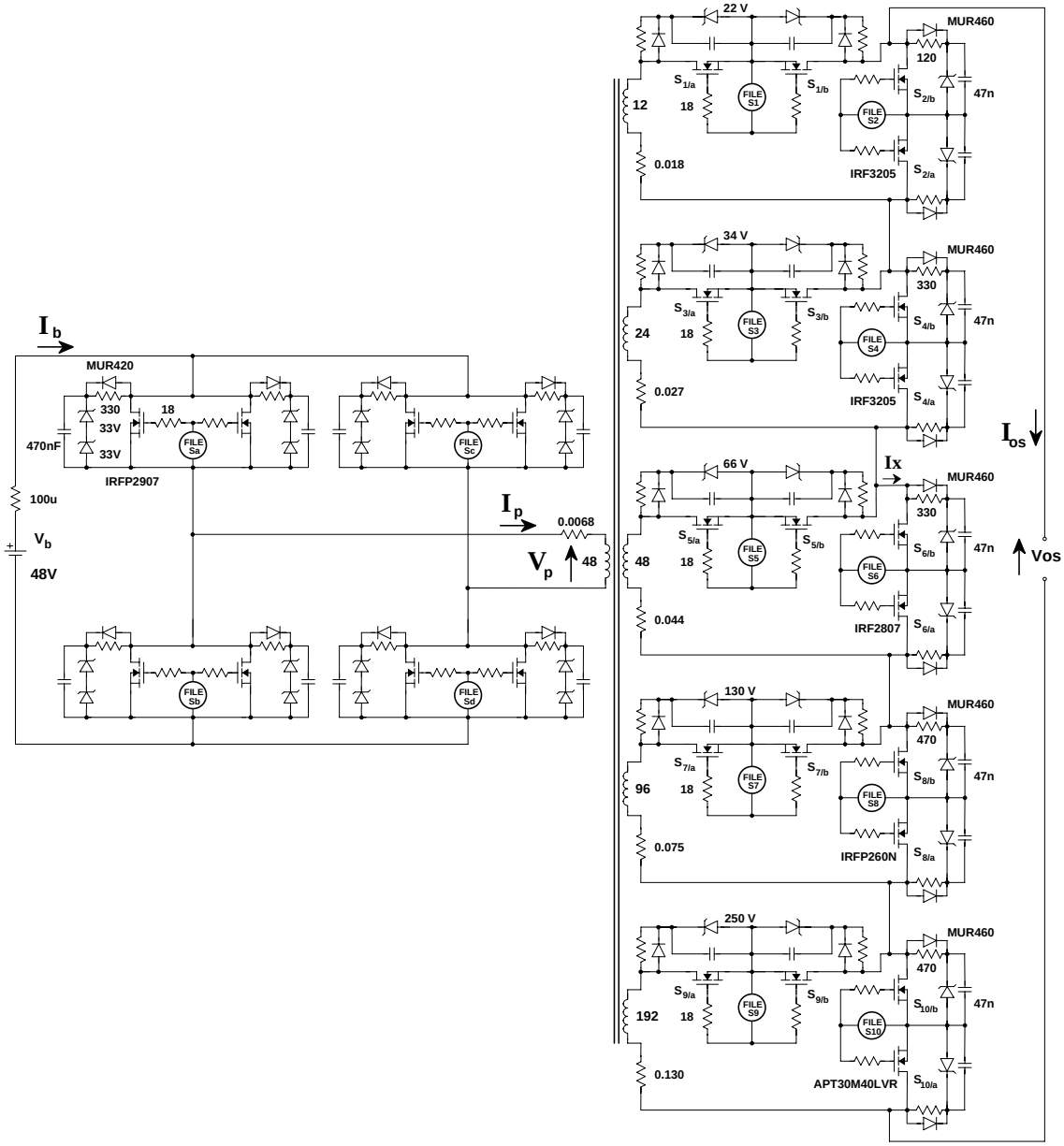


Figure 4.26 - Simulation schematic circuit: basic structure, without output filter.

Figure 4.27 shows the simulation result for the output-stage voltage (V_{os}) when a resistance of 52.9 Ω (load of approximately 1 kW) is connected across it. It is important to note that all simulations did not take into account wiring resistances, temperature elevation, transformer core losses and any other no-load consumption due control and auxiliary circuits. Thus, efficiency results obtained from simulation are expected to be higher than their practical values.

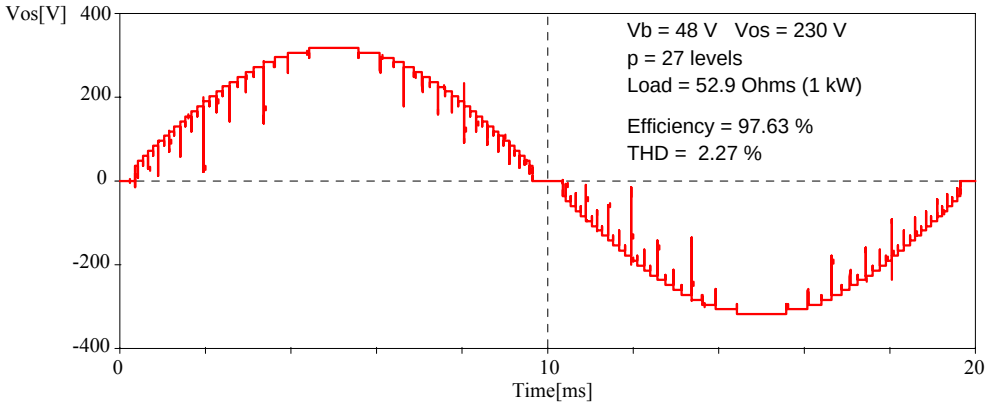


Figure 4.27 - Simulation result: output-stage voltage, without filter.

As can be seen in figure 4.27, the resulting output voltage presents high frequency voltage drops, which are associated to the dead times introduced between switch signals of a same output-stage.

4.8.3 *Simulation of the complete basic structure (resistive load)*

To minimize the undesirable high frequency voltage drops, a second order filter was connected between the converter output-stage and the load. The complete basic structure of the proposed converter is shown in figure 4.28 (compact schematic).

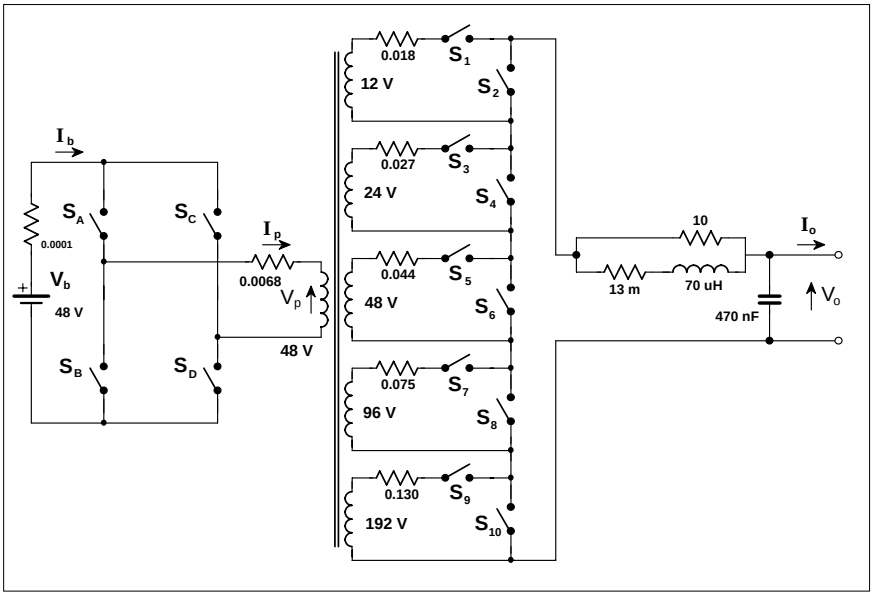


Figure 4.28 - Complete basic structure (compact schematic).

The filter parameters were design by a set of simulations (trial and error method, based on practical component values), and the final values are those showed in figure 4.28. Using this filter, cleaner output voltage can be achieved, as shown in figure 4.29. It is also important to note the output filter loss it not significant (0.6 W).

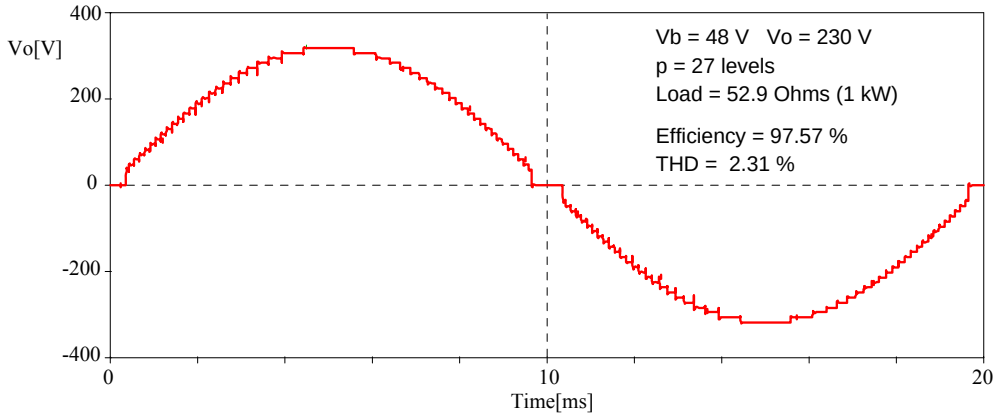


Figure 4.29 - Output voltage for the complete basic structure (P_o = 1 kW).

The battery current, shown in figure 4.30, presents high ripple and also high narrow spikes. Current ripple occurs due the natural power oscillation in the AC side, while current spikes are generated by quick charging of snubbers capacitors during switching transitions in the output-stage.

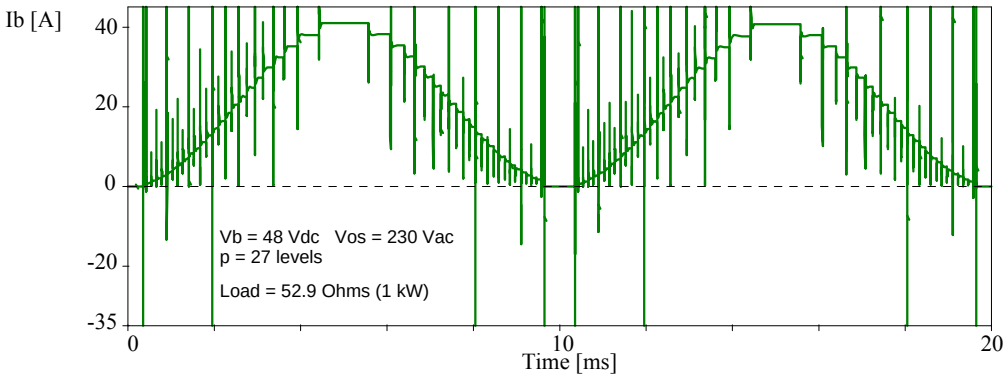


Figure 4.30 - Battery current for the complete basic structure (P_o = 1 kW).

Figure 4.31 shows a close view on a switching instant (turn off S_6 / turn on S_5), revealing that a current peak is generated just after the dead-time period. At this instant the switch S_5 is turned on, causing the quick charging of the snubber capacitor of $S_{6/b}$. During the peak interval, the battery current is almost equal to the 48 V secondary coil current, and the latter practically match I_x (refer to figure 4.26).

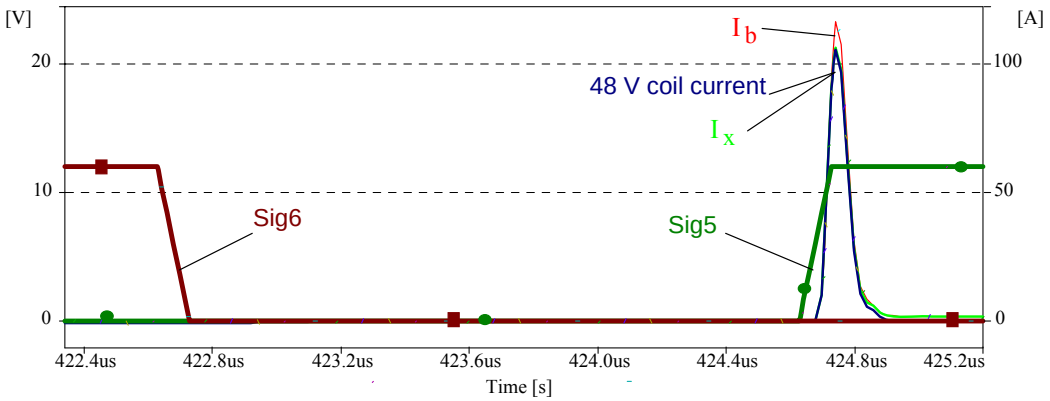


Figure 4.31 - Detail of the current peak during output-stage transition.

4.8.4 *Simulation under inductive load*

Figure 4.32 shows the voltage and current waveforms for inverter operation under pure inductive load. As can be seen, the output voltage is still comported and bi-directional operation is evident in both AC and DC sides.

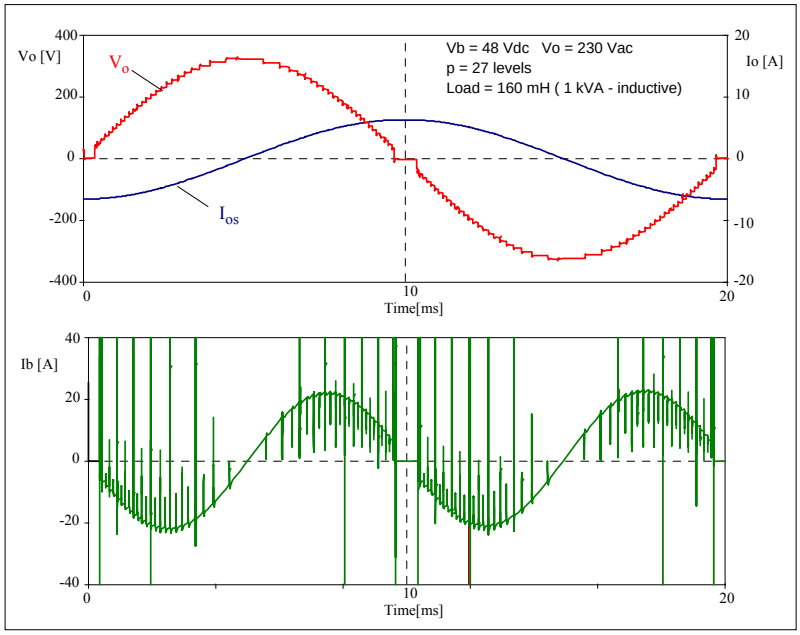


Figure 4.32 - Operation with pure inductive load.

As discussed in section 4.4.4, during dead-time intervals, some output-stage snubbers can be submitted to the total output-stage current if the inverter feeds an inductive load. An example of such condition is shown in figure 4.33, which shows the current and voltage across the zenner diode of switch $S_{2/a}$ and the output-stage current.

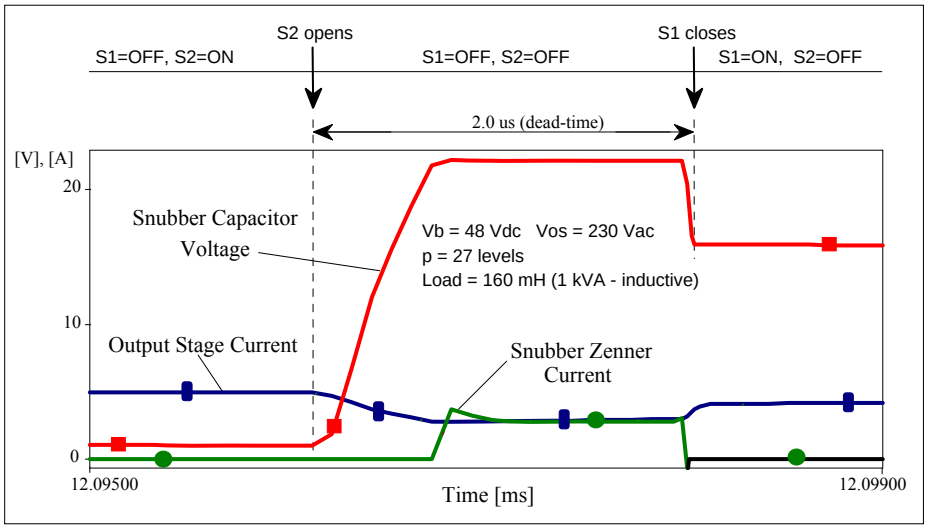


Figure 4.33 - Snubber operation under high inductive load.

As can be seen, during dead-time period, output-stage current charges the snubber capacitor until it reach zenner clamping voltage (22 V) and then output-stage current is fully conducted through the snubber zenner diode. It is important to note that, even under resistive load, this effect may occur due to the output filter inductor.

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5 Implementation

The implemented prototype is an unclosed but full-functional converter, which does not require any external circuits for its operation (except the batteries). This chapter describes the implemented prototype in detail.

5.1 Overall view and mechanical disposition

Figure 5.1 shows a block diagram of the complete system. As can be seen, the prototype has only two external electrical connections: the input from batteries and the output for the load. Another input/output present in the prototype is not an electrical connection, but it is a human-machine interface implemented by one keyboard and one LCD display.

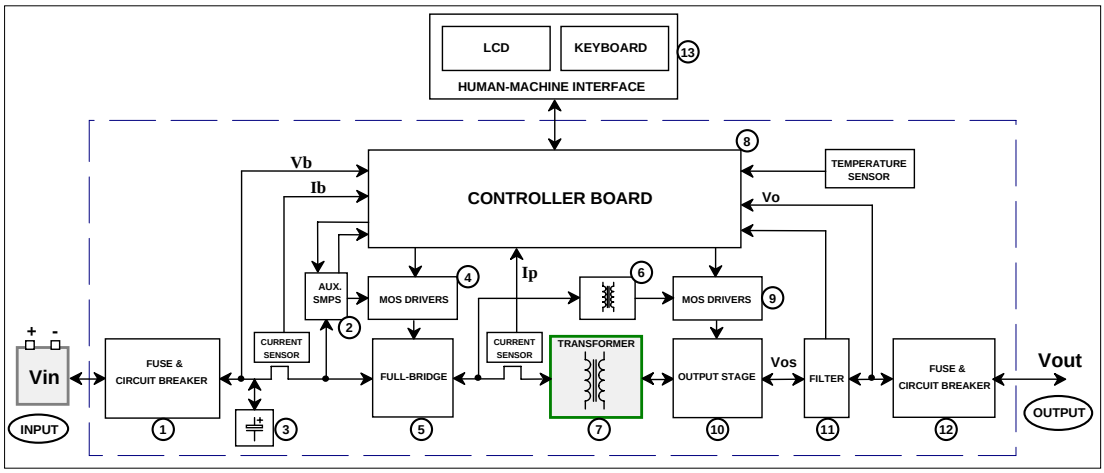


Figure 5.1 - Block diagram, showing all components.

Figure 5.2 shows a picture of the prototype, where it is possible to identify all components previously labeled in figure 5.1.

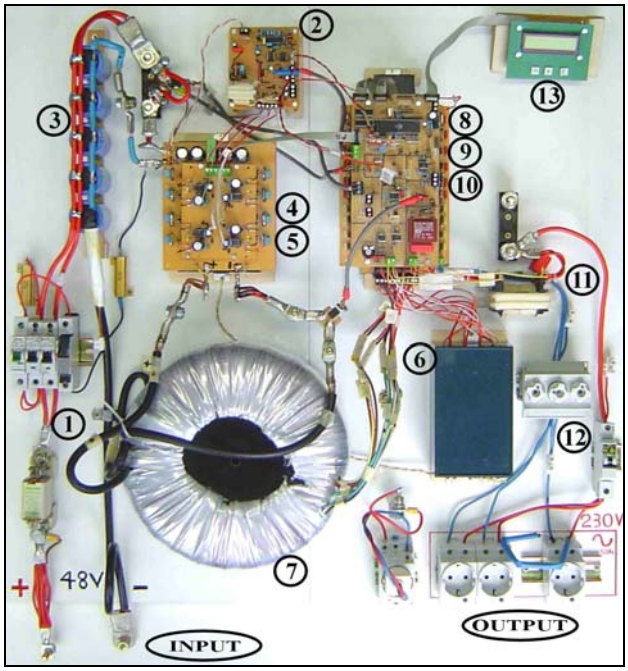


Figure 5.2 - Prototype top view.

In order to save space, two group of components were vertically mounted, as shown in figure 5.3. The H-bridge power board and its respective MOSFET driver board were mounted one above another, as shown in figure 5.3-left. At the output-stage module, a third layer, composed by the controller, was added as shown in figure 5.3-right.

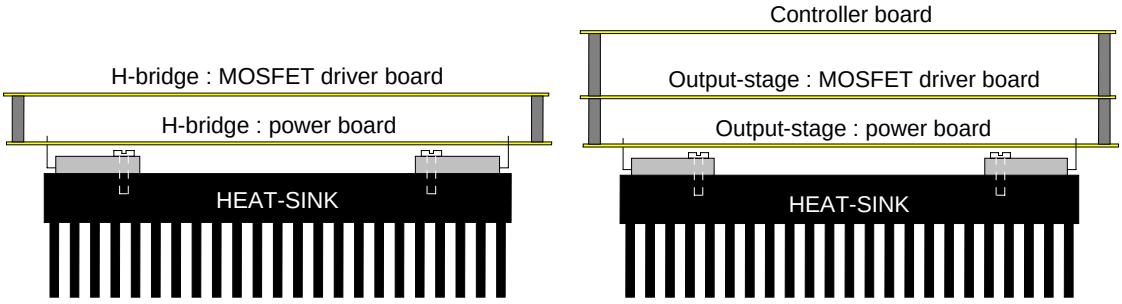


Figure 5.3 - Detail of the mechanical mounting: Right: H-bridge; Left: output-stage.

In the following sections each circuit is individually described.

5.2 Input front-end

The front-end circuit is composed by protections, filter capacitors and one current sensor, as shown in figure 5.4. The protections were designed to support overload conditions while the filter capacitors give more stability to the voltage applied to the H-bridge. In fact, these capacitors do not avoid high current fluctuations thought the battery when the converter operates with heavy loads. Although the current sensor can be used in the calculation of the input power, it is mainly used to trigger the over-current protection circuits. In the final experiments, it was necessary to add a shunt resistance in parallel with the current sensor in order to increase its full-scale value.

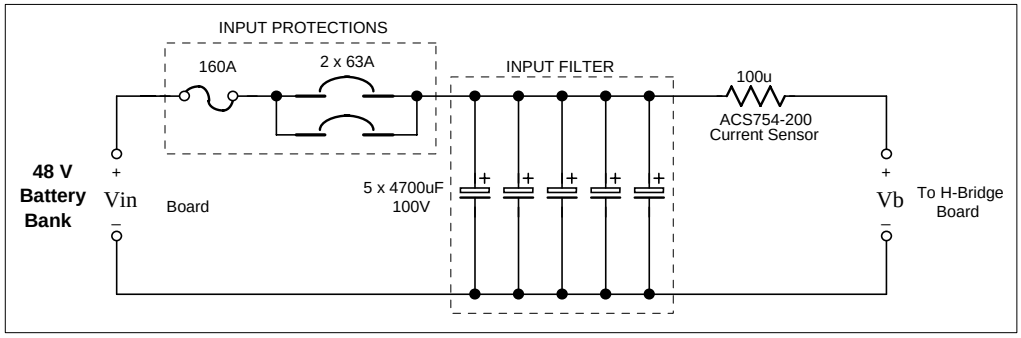


Figure 5.4 - Front-end circuit.

5.3 Auxiliary power-supply

Instrumentation, control and drivers require several regulated DC voltage sources with different values. Figure 5.5 shows the block diagram of the high-frequency Switch Mode Power Supply (SMPS) used to generate these voltage sources (complete schematic is found in Appendix E). The flyback topology was adopted because it can generate several isolated and regulated outputs while using only one transformer. Because the control circuits of the flyback converter require a DC voltage source to operate, a linear power supply was used to feed it at the startup instant. When the flyback converter is operating, the control circuits are feed by one of the regulated

outputs, thus eliminating the linear power supply losses and consequently reducing the overall converter no-load losses.

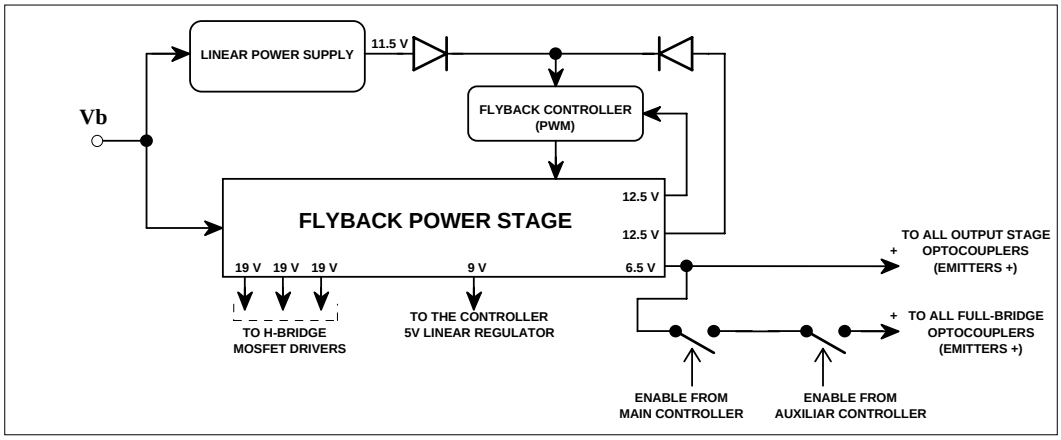


Figure 5.5 - Block diagram of the auxiliary power supply.

Three 19 V outputs are used to feed the four MOSFET drivers of the H-bridge (two of them have same reference), one 9 V output is used to feed the controller board and one additional 6.5 V output is used to feed the emitters of all driver optocouplers. In fact, these emitters could be feed by the regulated 5V power supply found in the controller board, but in this case higher losses would be expected (voltage drop from 9 V instead of 6.5 V). Another detail is found in the H-bridge optocoupler emitters source, where two switches were added in series, thus making possible to turn off all H-bridge drivers in case of abnormal situations.

5.4 MOSFET driver module

Figure 5.6 shows the MOSFET driver module used in the implemented prototype. As can be seen, it requires an isolated external voltage source and the driver signal is isolated by an optocoupler.

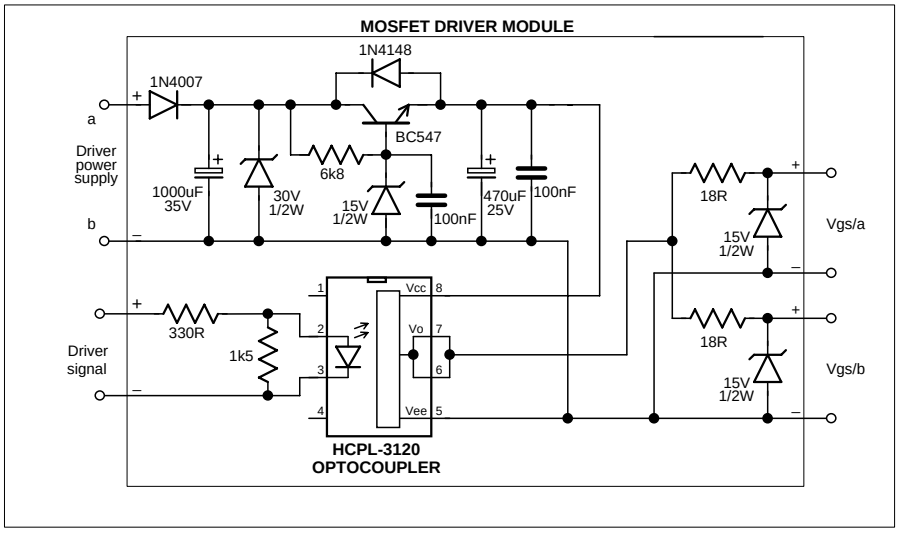


Figure 5.6 - Schematic circuit of one MOSFET driver module.

In order to reduce no-load losses, a low power voltage regulator was implemented based on one transistor and one zenner. Although the number of components is higher when

compared to a standard 7815 regulator, these discrete regulator present no-load consumption of about 1 mA while the latter consumes about 5 mA at no-load.

Two outputs, carrying the same signal, are available to feed two MOSFETs with same reference. For the H-bridge, these outputs are used to command two MOSFETs in parallel and at the output-stage they are used to command two MOSFETs in anti-series connection.

5.5 H-bridge and transformers

The H-bridge inverter board schematic and the devices directly connected to it are presented in the electrical diagram shown in figure 5.7. Some filter capacitors were mounted in the H-bridge board in order to absorb the high frequency current peaks during switch transitions. As can be seen, the output of the H-bridge is connected to the main transformer thought a current sensor that is used by the controller to detect transformer-unbalancing. Also an auxiliary transformer is connected to the H-bridge output in order to provide ten isolated power sources to feed the output-stage drivers.

In fact, three solutions could be used to implement the power supplies of the output-stage drivers: in the auxiliary SMPS, as ten additional coils in the main transformer or through an isolated low frequency transformer. The last option was adopted because it was easy to implement and it is robust.

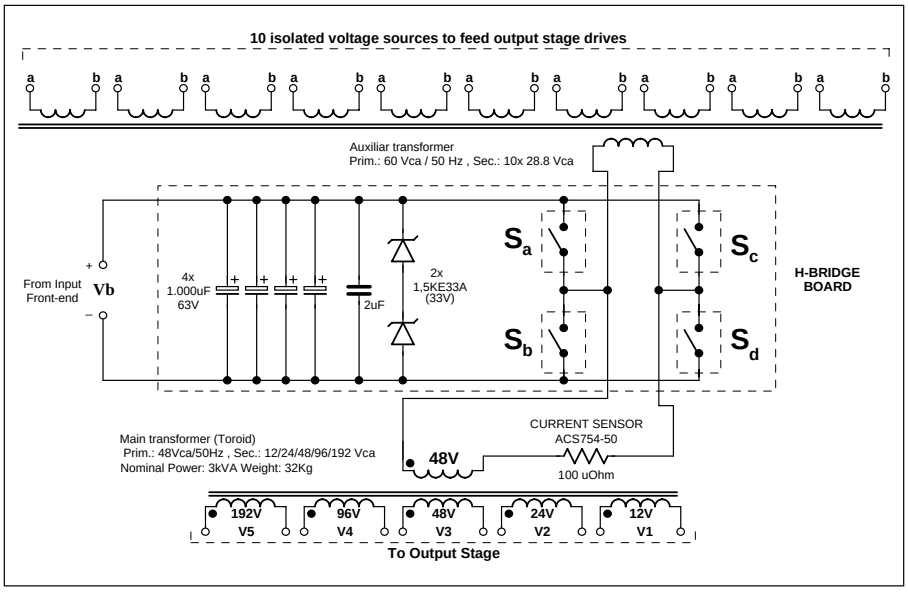


Figure 5.7 - Compact schematic of the H-bridge module and transformers.

Although the H-bridge switches does not require an isolated driver module, all drivers used in the prototype was of the type shown in figure 5.6. It is important to note that such isolated driver is more expensive and have higher consumption than conventional non-isolated bootstrap drivers. On the other hand, it is more robust against noise and it is expected that it can provide improved reliability.

Figure 5.8 shows the complete circuit of one H-bridge switch module. As can be seen, two IRFP2907 MOSFETs (75 V, 209 A, 4.5 mΩ) are connected in parallel to compose each single module, reducing conduction resistance and consequently conduction losses. In this case, because of the switching frequency is low (50 Hz), no significant increase in switching losses occurs due to the use of two switches in parallel.

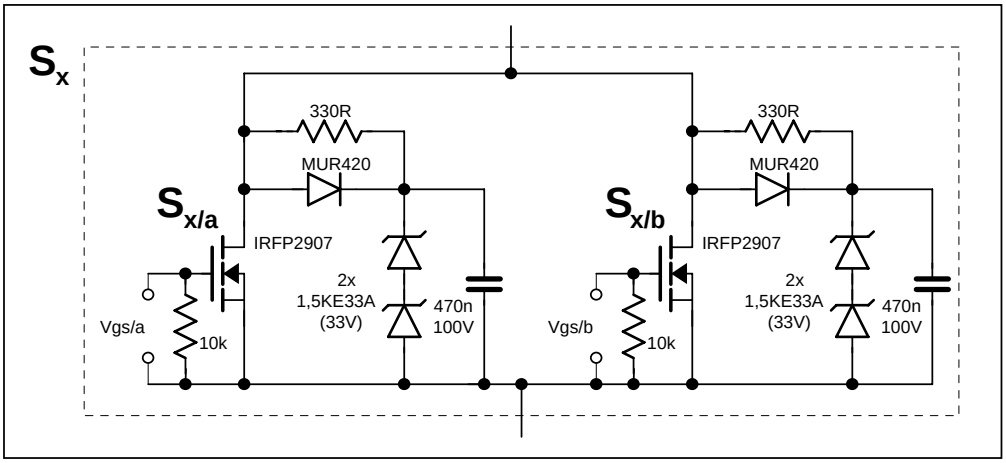


Figure 5.8 - Schematic circuit of an H-bridge switch-module.

As can be seen in figure 5.8, rugged snubbers were added to each switch to decrease the dv/dt ratio during the switch turn-off, thus increasing reliability. These snubbers are also fundamental to the balance-control mechanism described in section 4.4.

5.6 Output-stage

The output-stage is composed by five modules with the same structure shown in figure 5.9. Each module is connected to its respective main transformer coil and the outputs of all modules are connected in series. Each switch is protected by a passive snubber and zenner diode.

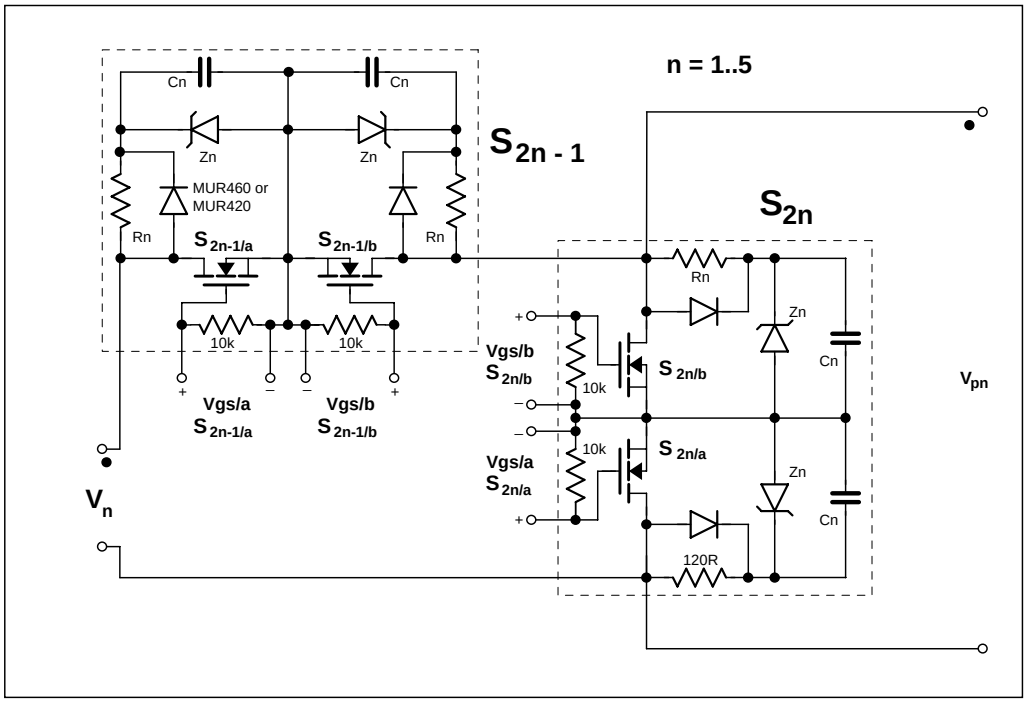


Figure 5.9 - Schematic circuit of one output-stage module.

The values of the specific components for each module were already presented in section 4.7.4.

5.7 Controller

A block diagram of the controller board is shown in figure 5.10 and the complete circuits are found in appendix F. The 5 V linear regulator was incorporated to the main controller board (instead of integrated to the auxiliary SMPS) in order to minimize interference and increase reliability. The analog interface circuits are composed by the measurement circuits and also by some protections at each analog input pin of the main microcontroller. An interface composed by two transistor arrays was used to connect the microcontroller pins to the optocoupler emitters of all MOSFET drivers.

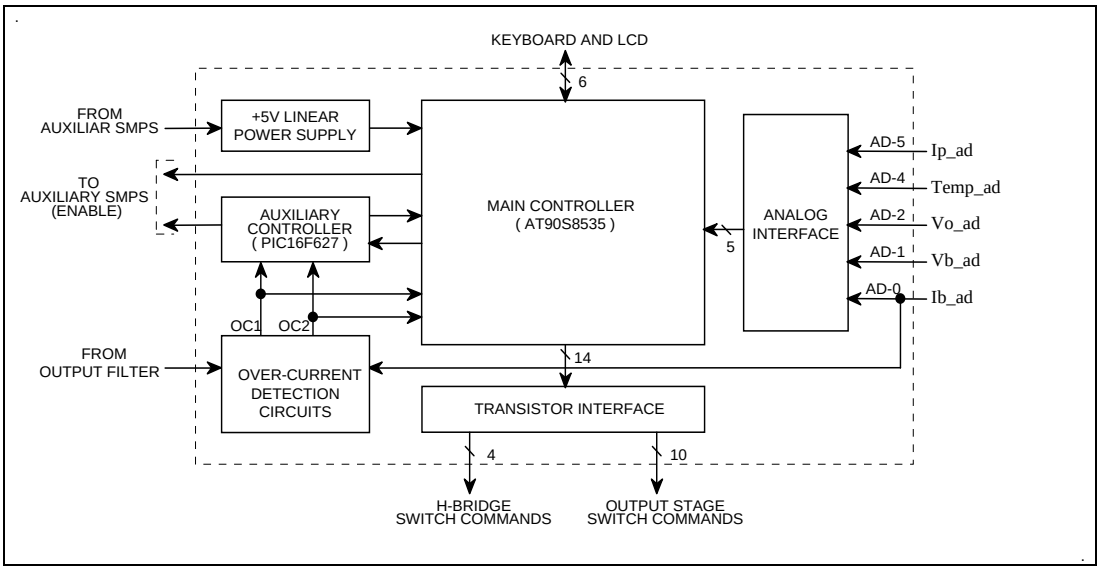


Figure 5.10 - Block diagram of the controller board.

The controller is based on one 8-bit AT90S8535 microcontroller (running at 11.0592 MHz) from ATMEL [96]. The control program was developed in C language and the microcontroller was programmed by an In Circuit Programming (ICP) interface, thus reducing the developing time. It should be mentioned that the program memory of the main controller was exhausted at the final firmware version and it is recommended for future works the use of other microcontroller with larger program memory.

An auxiliary microcontroller was used to ensure safe shut-down of the power stage in case of main microcontroller failure. In fact, if either of the microcontrollers stops working, then the remainder will turn off the converter power stage by cutting off the power supply of all optocouplers that drive the H-bridge switches.

5.7.1 Measurement circuits

The measurement circuits, shown in figure 5.11, are composed by sensors and conditioner circuits that are connected to the Analog to Digital (A/D) converter inputs of the main microcontroller. The battery voltage is conditioned basically by a simple resistive voltage divider, as shown in figure 5.11(a).

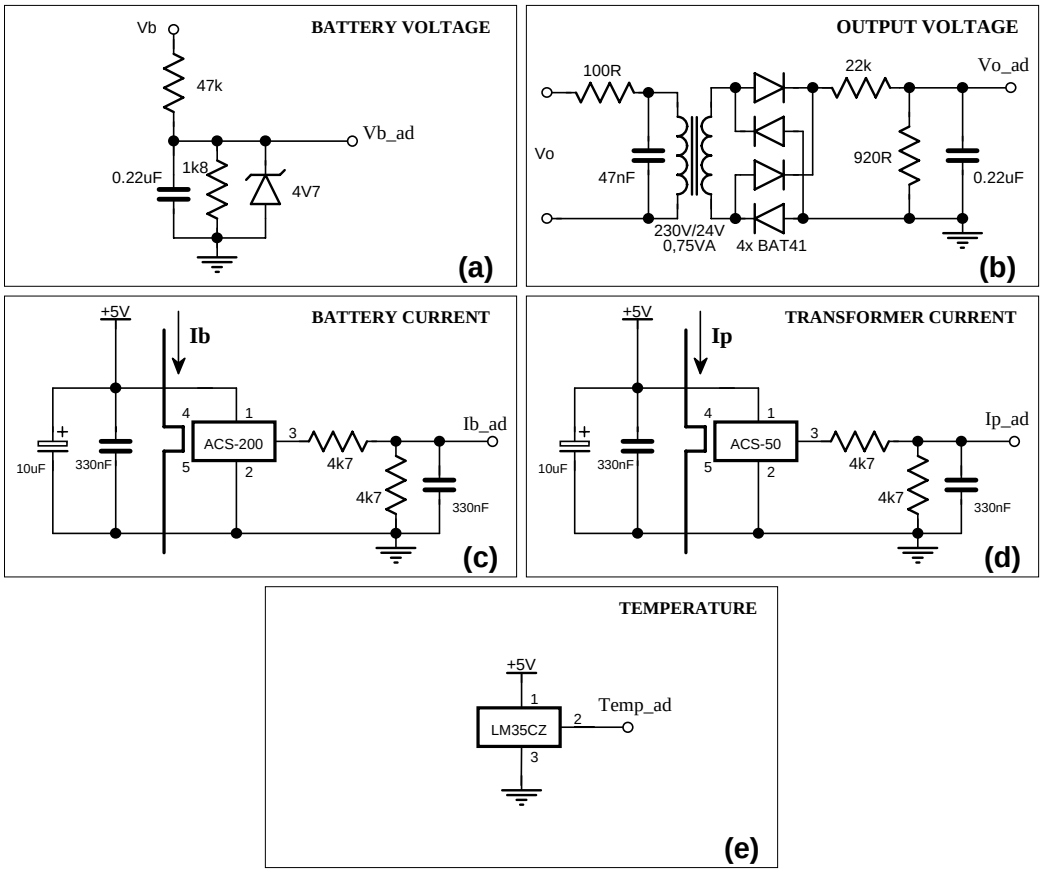


Figure 5.11 - Schematic of the measurement circuits.

The circuit used to monitor de output AC voltage is shown in figure 5.11(b), where a conventional low power transformer is used to provide isolation and also to reduce the voltage magnitude. It should be noted that the resultant voltage that is applied to the A/D converter is a rectified full-wave voltage. In fact, the microcontroller program makes several measurements during one cycle in order to calculate an approximation of the output voltage RMS value.

The circuits used to measure the battery current and transformer current are electrically isolated by hall-effect sensors [97], as shown in figures 5.11(c) and 5.11(d). These sensors are 5-terminal devices, where the input-current terminals are modeled as an equivalent 100 uΩ resistance throughout the measured current must flow (see figures 5.4 and 5.7). It should be noted that these sensors require only a single power supply of 5 V while make possible to measure the current in both directions (an offset of 2.5 V is provided at its output). These characteristics allowed simplifications on the controller power supply and also on the required analog conditioner interface, thus reducing component count.

Finally temperature is measured by a precision integrated-circuit temperature sensor (LM35CZ), and any conditioner circuit is required, as shown in figure 5.11(e).

5.8 Output filter and protections

The output-stage is connected to the load through the circuit shown in figure 5.12. This circuit is composed by an output filter and over-current hardware protections. Although the output filter inductor was implemented with a high frequency core, for future implementations, filters built of low frequency cores may be experimented.

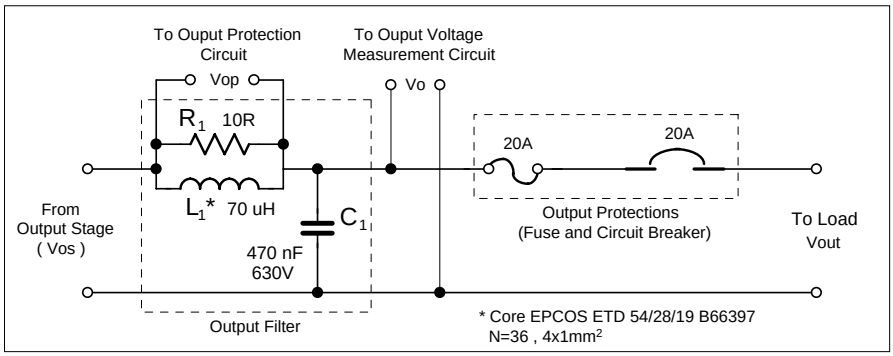


Figure 5.12 - Schematic circuit of the output filter and protections.

6 Experimental Results

Several experiments were done in order to evaluate the steady state and dynamic characteristics of the implemented prototype. In these experiments, measurement of power became somehow critical because of the high values of efficiency that had to be calculated; therefore high precision instrumentation was required.

Efficiency measurements were done using a high precision power analyzer instrument (NORMA D6000 of LEM Instruments [98]). This device has a specified precision of less then 0.1% for power measurements. Voltage and current waveforms were acquired using a Tektronix four channel digital oscilloscope. Figure 6.1(left) shows a picture of the experimental setup, where these equipments can be observed.

All[1] experiments were done at room temperature between 23 ºC and 30 ºC (Kassel - Germany - Summer 2005). Long-time experiments (characteristic curves tracing) were done using ISET Virtual Battery installed in DeMoTec, which is shown in figure 6.1(right). Other experiments, such as load startups, were done using a battery bank of 48 V.

Figure 6.1 - Left: Experiment setup, showing instrumentation; Right: ISET Virtual Battery in DemoTec.

In order to checkout the implemented prototype behavior under practical load condition, the set of loads shown in figure 6.2 were experimented.

Figure 6.2 - Set of loads experimented with the prototype.

[1] Exception is the experiment shown in figure 6.14, which was done in winter, at room temperature of about 18 ºC.

6.1 Output voltage analysis

As an inverter is essentially a voltage source at its output, the first parameter to be analyzed is its output voltage waveform, which is showed in figure 6.3.

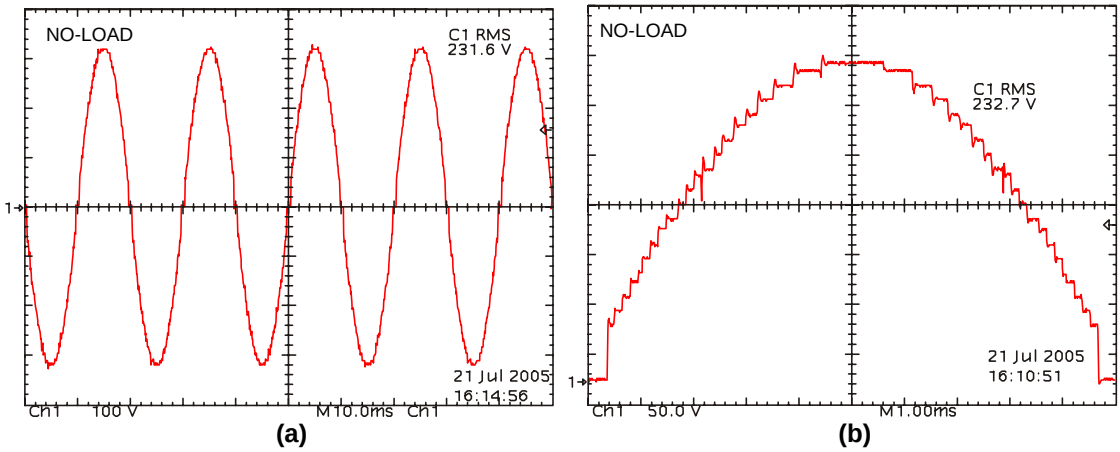


Figure 6.3 - (a) No load output voltage (five cycles); (b) No load output voltage (zoom: half cycle)

As can be seen, the output waveform approximates a perfect sinusoidal shape, apart from the distortions near zero crossing. As was explained in section 4.4, these distortions correspond to a fixed time of 700 μs where the output voltage is forced to be zero, and it is used to control transformer-unbalancing.

Because voltage steps are so small, it is difficult to identify at figure 6.3(a) each step of the multilevel waveform. In Figure 6.3(b), it is possible to observe all steps in detail. In fact, some steps could be omitted, due to the hold-on-at-zero interval, resulting in a relatively high initial step, as discussed in section 4.5.3.

An even closer zoom can be observed in figures 6.4(a) and 6.4(b), which corresponds to the no-load and 2 kW resistive load operations, respectively.

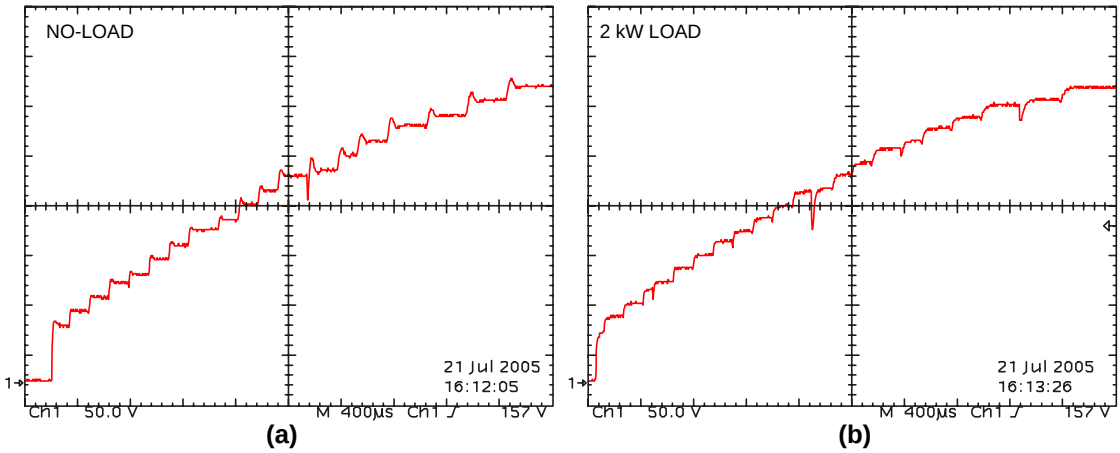


Figure 6.4 - Close-up at output voltage waveform: (a) No-load; (b) Load of 2 kW.

As can be seen in figure 6.4(a), at no-load condition, it is found voltage spikes near each step transition, which are due to the second-order characteristic of the filter (this fact shows the importance of the 10 Ω resistance in parallel with the filter inductor). On the other hand, when the inverter is under load, these voltage spikes are minimized (or even eliminated) due to the additional dumping introduced by the load.

As discussed in section 4.5.2, the RMS value of the output voltage can be adjusted by varying the number of output levels. As can be seen in figure 6.5(a), where only the first 16 levels are used, the output voltage is equal to only 130 V. When the number of levels is increased to 31, then the output voltage is increased to 250 V, as shown in figure 6.5(b).

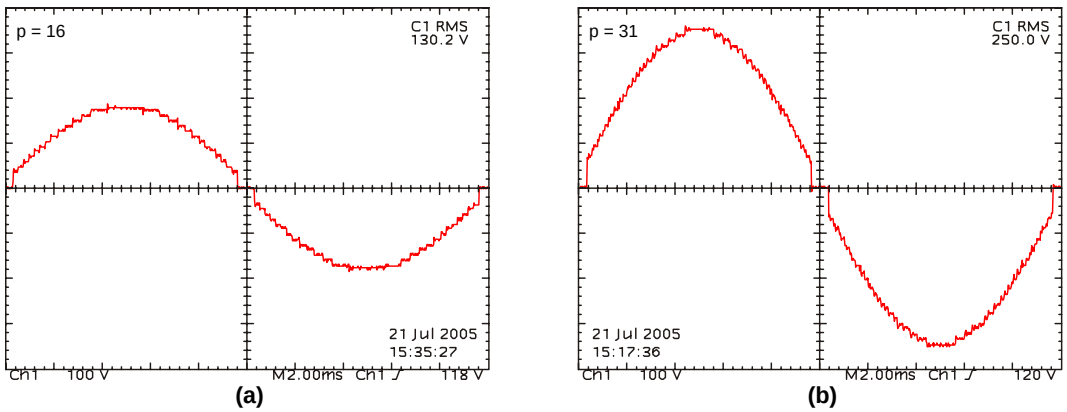


Figure 6.5 - No load output voltage: (a) p = 16; (b) p = 31.

Figure 6.6(a) shows the output voltage RMS value versus p (V_b = 42.9V). As expected, this characteristic is linear.

Under normal operation condition (automatic mode), the implemented controller adjusts the number of output levels in order to keep the output voltage close to its nominal value of 230 V_{CA}. Because of the number of levels is finite, the output voltage presents some discontinuities as the input voltage is varied over a wide range, as shown in figure 6.6(b).

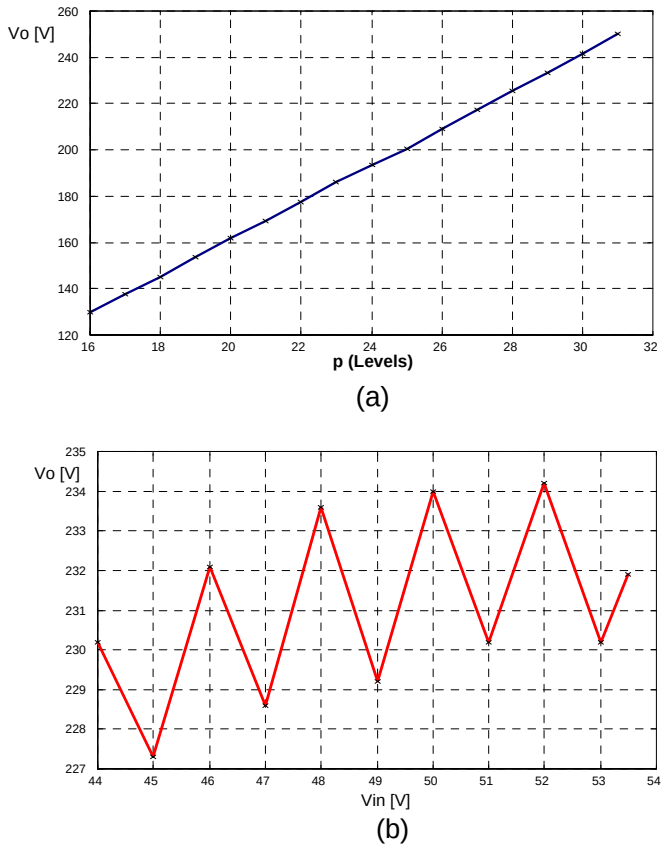


Figure 6.6 - (a) Output voltage versus p; (b) Output voltage versus input voltage (no-load)

The influence of the load on the output voltage regulation (automatic mode) can be observed in figure 6.7, which shows the output voltage versus load power characteristic for battery voltages of 44, 48 and 52 V. As can be seen, in the worst case, a voltage drop of about 6% occurs for a load of approximately 3.4 kW and input voltage of 44 V.

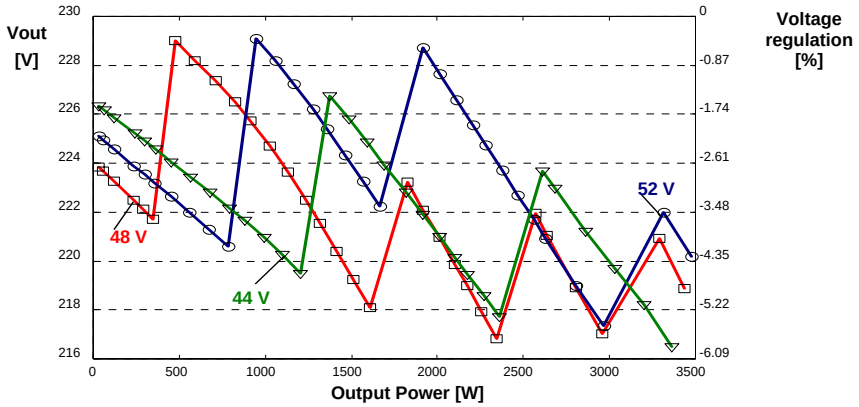


Figure 6.7 - Output voltage x output power (V_b = 44, 48 and 52V) - automatic mode.

In addition to voltage regulation, frequency regulation and total harmonic distortion are the other parameters of major importance of a voltage source. In the implemented prototype, frequency stability was not critical because it was digitally generated and based on a crystal oscillator. Nevertheless, frequency deviations can only occur in case of defects and the analysis of such remote condition is out of the scope of this work.

Figure 6.8(a) shows the estimated and experimental values of the THD (calculated up to 50th harmonic) for the output voltage (no-load) as a function of the number of output levels. As can be seen, total harmonic distortion is lower then 4% for any p between 16 and 31.

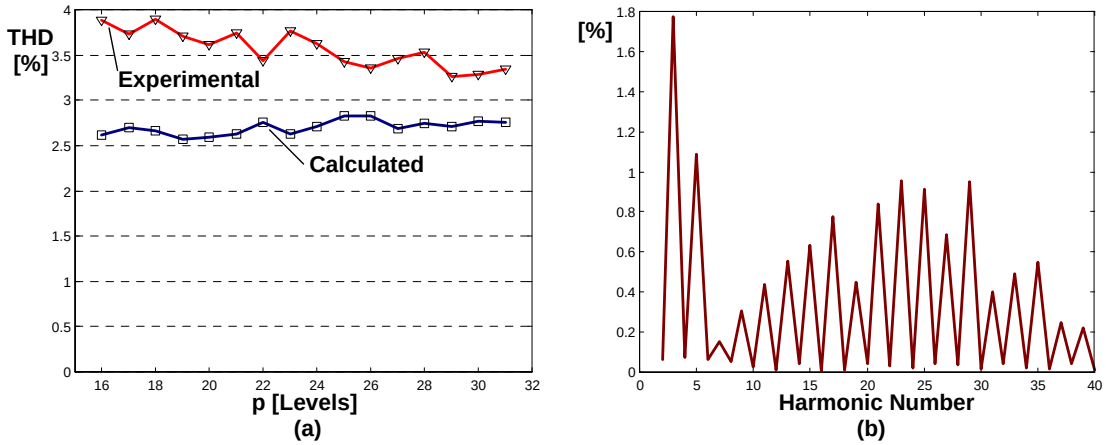


Figure 6.8 - (a) THD x p; (b) Spectrum for the waveform with p = 31.

It is also interesting to note that, for the experimental data, THD only slightly decreases with the maximum used level. In this case, the introduced hold-on-at-zero interval is the main cause of distortion and the number of levels presents low influence on the final value of the THD. As shown in Figure 6.8(b), only odd harmonics have significant contribution, as expected.

6.2 Switching waveforms

Analysis of switching waveforms is important to check out occurrence of stress in switches. Critical instants occur when the switches are switched off because high dv/dt and over-voltage conditions may appear.

Figure 6.9 shows the voltage across all H-bridge switches (no-load). As can be seen, these waveforms have good aspect and no voltage spikes are found. Short transients presented in the falling edge of switch S_d and rising edge of switch S_c are due to the transformer-unbalancing control, as explained in section 4.4.

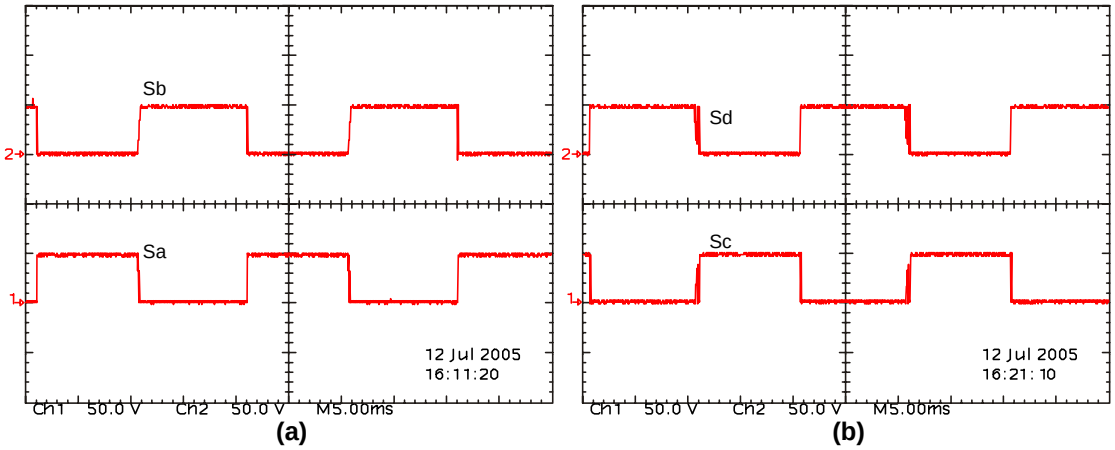


Figure 6.9 - (a) Voltage at H-bridge switches S_a and S_b;
(b) Voltage at H-bridge switches S_c and S_d.

Voltages across output-stage switches present also good behavior as can be seen in figure 6.10 (no-load), where the voltages at switches $S_{1/a}$, $S_{2/a}$ and $S_{9/a}$ are showed.

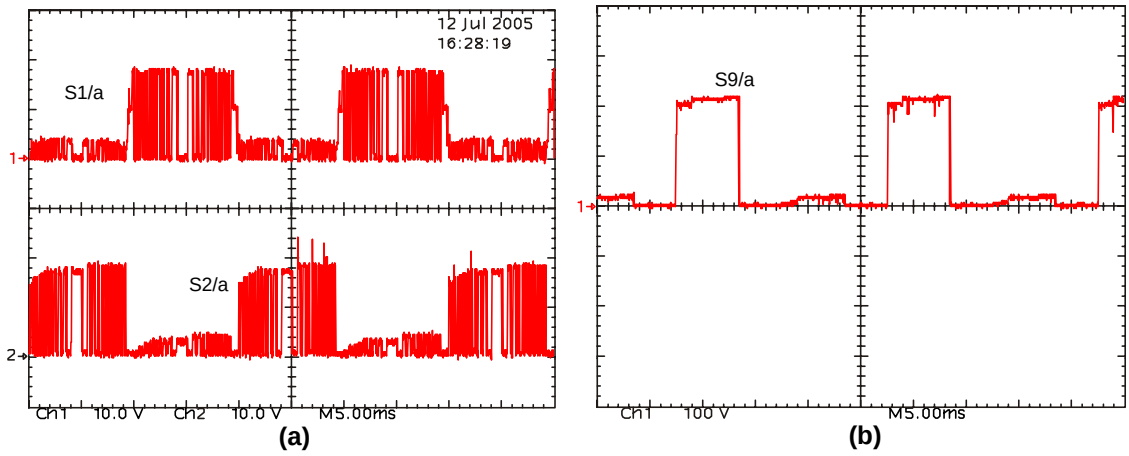


Figure 6.10 - (a) Voltage at output-stage switches $S_{1/a}$ and $S_{2/a}$;
(b) Voltage at output-stage switch $S_{9/a}$.

Figure 6.11 shows close views at the turn-off instants of $S_{1/a}$ and $S_{9/a}$ (no-load). Although some voltage spikes are presented, they are below the rated V_{ds} voltage of their respective MOSFETs (peak of 55 V for switch $S_{1/a}$ / V_{ds} = 55 V; peak of 260 V for switch $S_{9/a}$ / V_{ds} = 300 V). In figure 6.11(b), it is also possible to observe how the snubber circuit of switch $S_{9/a}$ introduces smoothness to its turn-off characteristic.

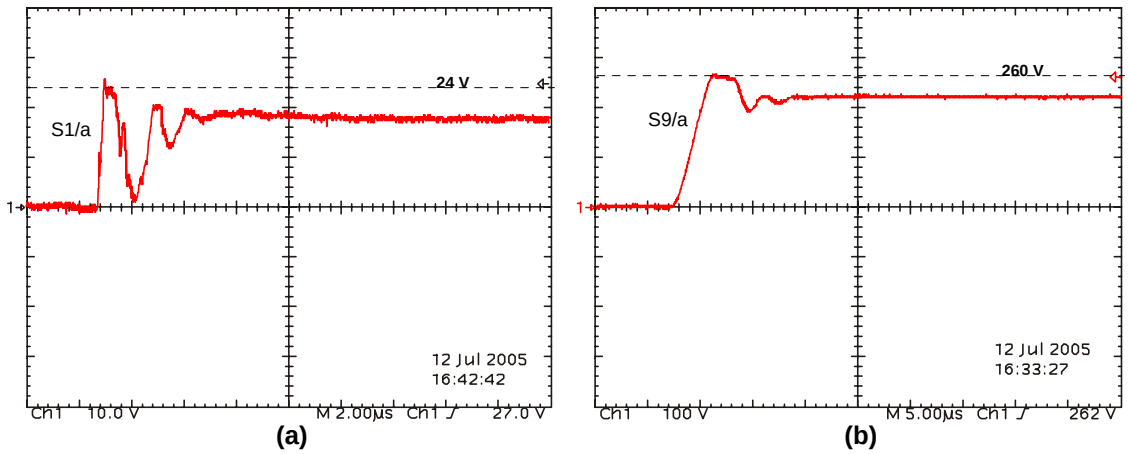


Figure 6.11 - (a) Transient at switch $S_{1/a}$; (b) Transient at switch $S_{9/a}$.

As discussed in section 4.6.4, the dead-time between complementary switches was introduced to avoid short-circuits at switching transitions. These dead times are equal to approximately 2 µs for the H-bridge switches and also to the output-stage switches. In consequence, the output-stage waveform presents quick drops, as can be seen in figure 6.12(a). However, thanks to the output filter, the output voltage delivered to the load is almost free of these distortions, as shown in figure 6.12(b).

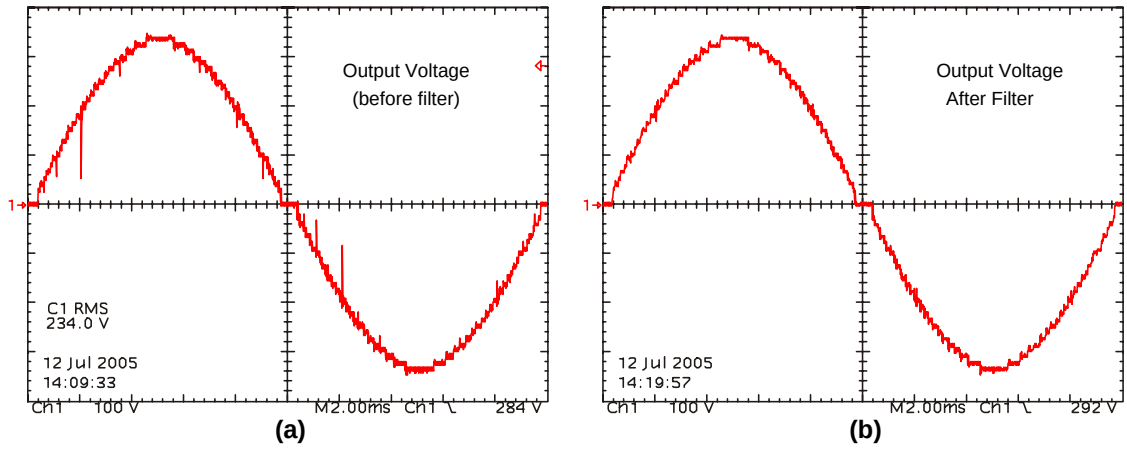
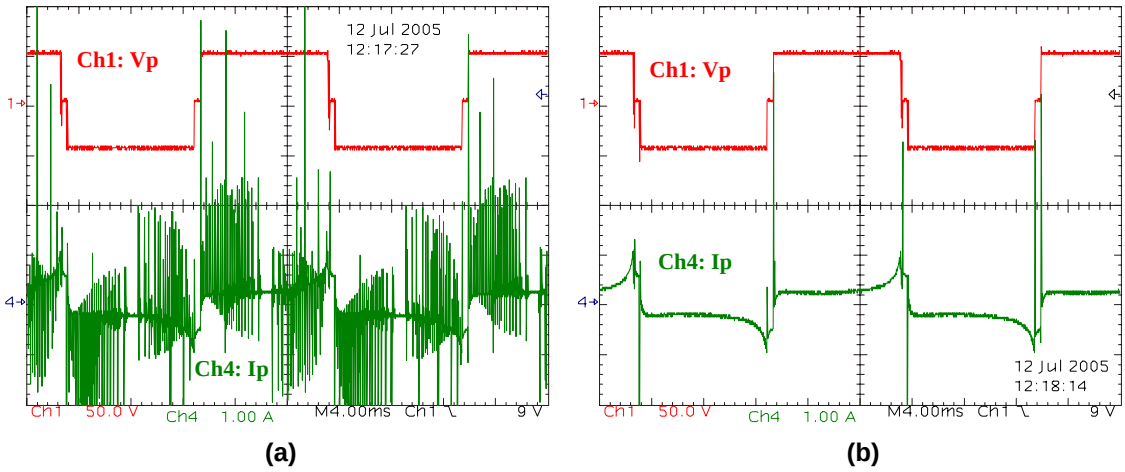


Figure 6.12 - (a) Output voltage before filter; (b) Output voltage after filter.

As predicted by the simulation presented in section 4.8.3, the transformer primary current present narrow spikes due to the quick charging/discharging of the snubber capacitors of the output-stage switches, what can be verified in the waveform shown in figure 6.13(a). If the output-stage is turned off while maintaining the H-bridge under normal operation, then most spikes disappear, as shown in figure 6.13(b).



(a) **(b)**

Figure 6.13 - (a) Voltage and current at the transformer primary (normal operation);
(b) Voltage and current at the transformer (output-stage off).

According to sections 4.6.4 and 4.8.4, during dead-time periods of the output-stage switches, total load current may flow thought switch snubbers (even thought the switches, operating under controlled avalanche). Figure 6.14 illustrates such situation, when the prototype makes the startup of a vacuum cleaner (inductive load). As can be seen, just after $S_{5/a}$ (V_{ds} = 75 V) is turned off, relatively high current circulates through the zenner diode of $S_{5/a}$ snubber circuit and the initial clamping voltage (around 80 V) exceeds $S_{5/a}$ rated voltage. However, taking into account the amount of energy that is dissipated (roughly, 1.6 mJ = 20 A x 80 V x 1 µs), it is expected that such condition may not be so critical, since $S_{5/a}$ is rated to repetitive avalanche energy of 23 mJ and the total value of 1.6 mJ is even shared between $S_{5/a}$ and the zenner diode.

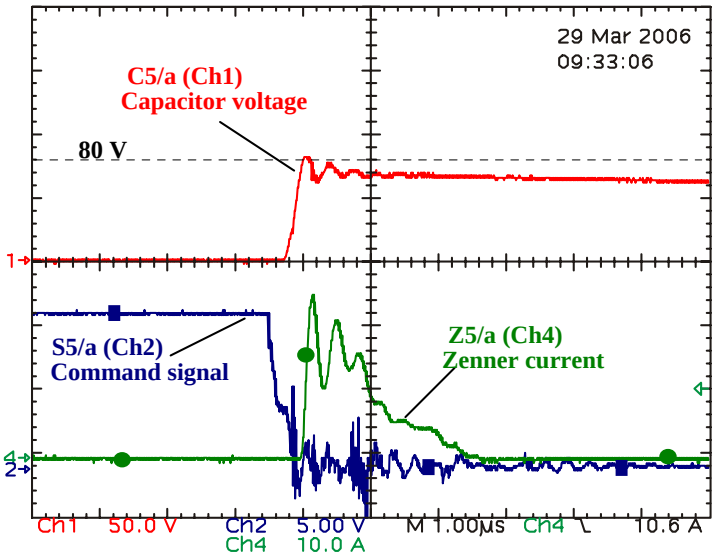


Figure 6.14 - Command signal of switch $S_{5/a}$ and voltage/current at the capacitor/zenner of its snubber circuit.

It is also important to note that the dv/dt stress applied to $S_{5/a}$, which can be estimated in 0.4 V/ns (80 V/200 ns), may not be critical since typical values are in the range of several V/ns (depending on the switch technology, rated voltage and current).

6.3 Transformer-unbalancing control

The developed mechanism to control transformer-unbalancing makes use of the hold-on-at-zero intervals, as described in section 4.4. The two control actions involved in this process can be observed in figures 6.15(a)-6.15(d), which shows the evolution of the corrections as the converter feeds half wave loads of increasing power. In these examples, the voltage drop at the transformer primary voltage is compensated by replacing part of the hold-on-at-zero interval for additional positive intervals.

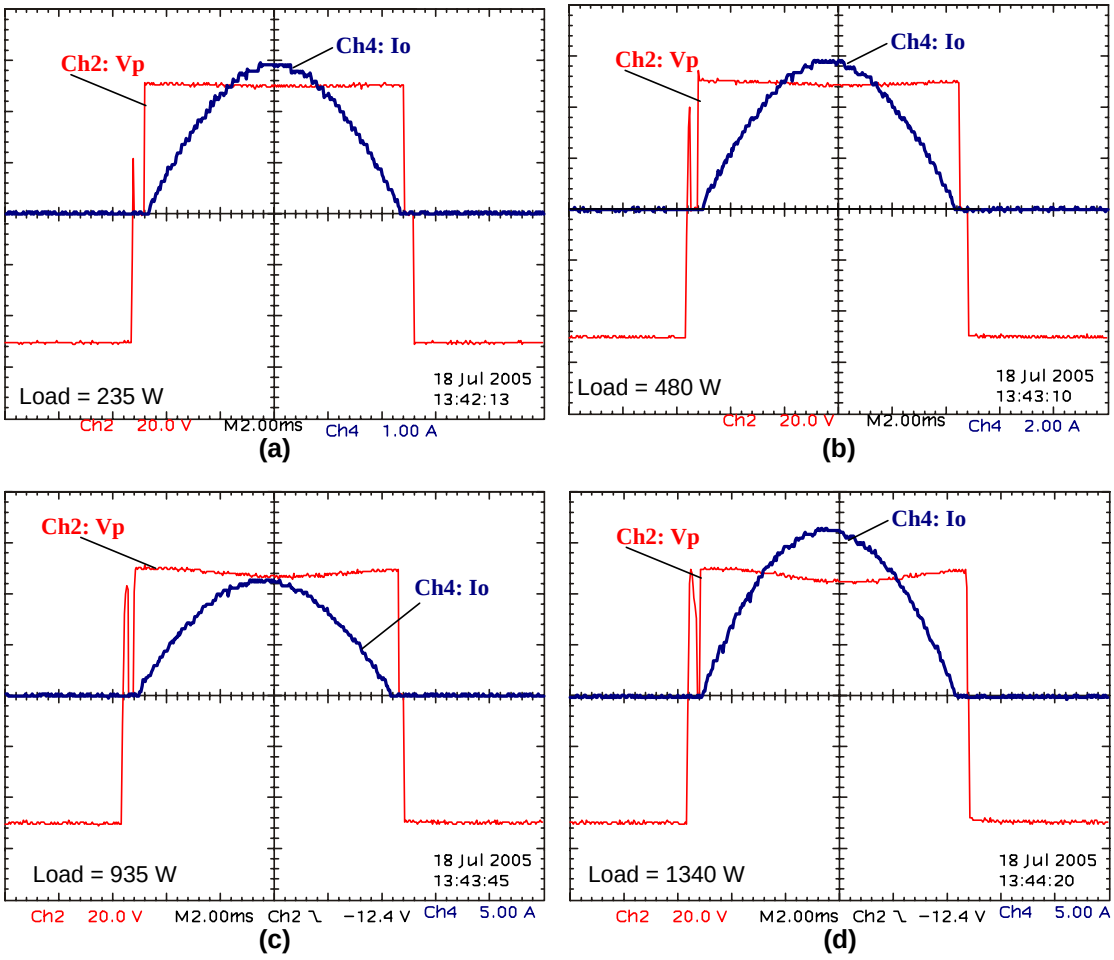


Figure 6.15 - Voltage at the transformer and output current under half wave resistive loads of: (a) 235W (b) 480W (c) 935W d) 1340W.

Looking at figure 6.15(d), it is possible to conclude that for the 1340W load the correction reaches its limit and further load increase may not be compensated.

In the implemented prototype, it was possible to select any of the two current sensors (one at the H-bridge input and the other direct in series with the transformer) to feed the transformer-unbalancing controller. Experiments showed that the use of the sensor direct on the transformer presents better performance, as showed in figure 6.16. This behavior can be attributed to two factors: first, the sensor at the input of the H-bridge has lower sensibility (higher full-scale value); second, the capacitors located at the H-bridge board introduce distortion on the current measurements and the controller is affected.

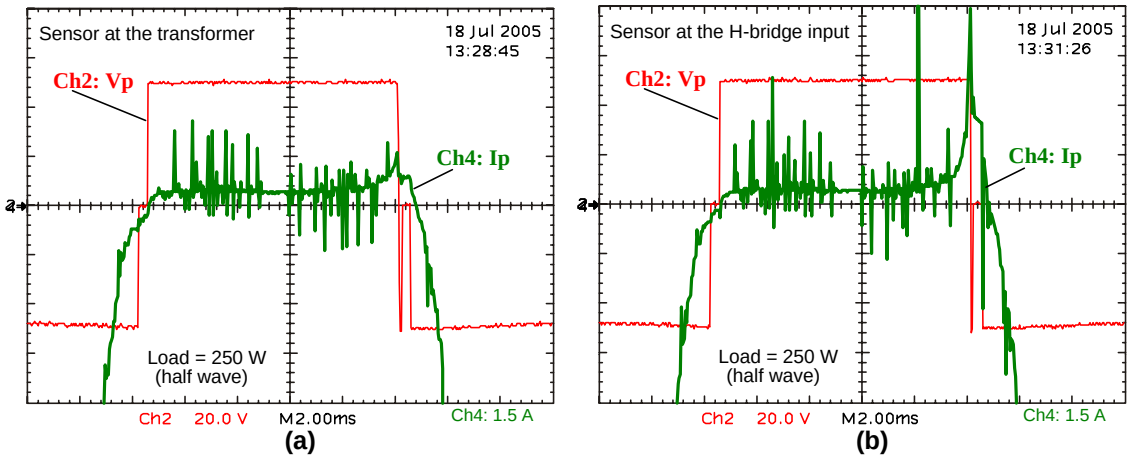


Figure 6.16 - Voltage and current at the transformer primary for different balance-sensor position:
(a) Sensor at transformer (250W half-wave load);
(b) Sensor at H-bridge input (250W half-wave load).

The floating period described in section 4.4.5 can be clearly observed in figure 6.17. The six intervals described in figure 4.11 can be clearly identified in figure 6.17(a), which shows a situation where the magnetizing current peak is relatively low. On the other hand, when the transformer-unbalancing control reaches its limit, the transformer start to saturate and the falling edge of V_p is almost vertical, as can be observed in figure 6.17(b).

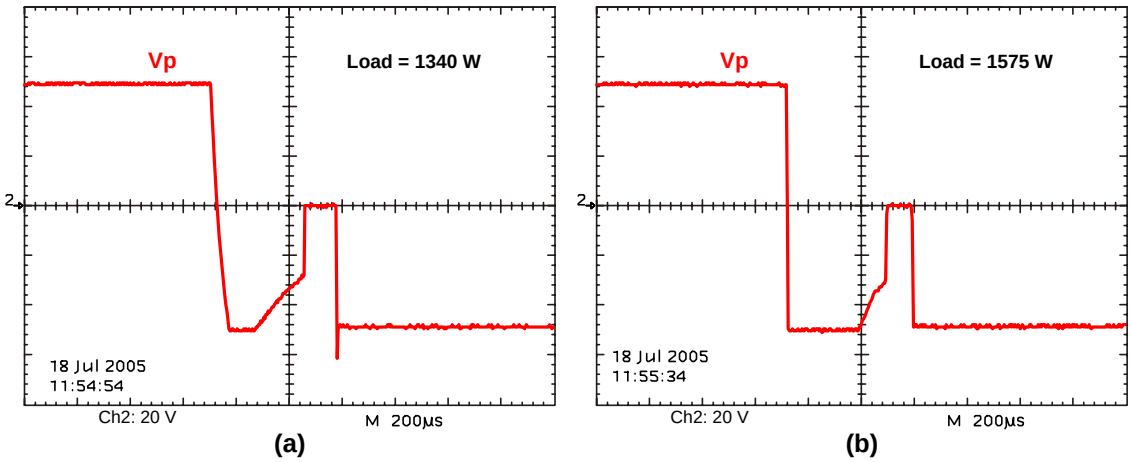


Figure 6.17 - (a) Control action-1 (P_o = 1340 W); (b) Control action-1 (P_o = 1575 W).

Because the magnetizing current peaks depend on the converter input voltage, the floating interval of the transformer-unbalancing control mechanism is also altered when the input voltage changes. Figures 6.18(a) and 6.18(b) show close-ups at the floating interval for input voltages of 48 V and 44 V, respectively. In this experiment, the extension interval of the proposed technique was removed so all necessary correction had to be done in the floating interval. In this case, the necessary compensation time is strongly influenced by the magnetizing current peak and consequently by the input voltage value.

It is also important to note that the beginning of the floating interval has an opposite contribution to the correction process and this fact gives origin to a fine self correction of the magnetizing current peak. In other words, if the magnetizing current peak increases, then voltage polarity changes more quickly, decreasing the negative interval while increasing the correction until a stable condition is reached again.

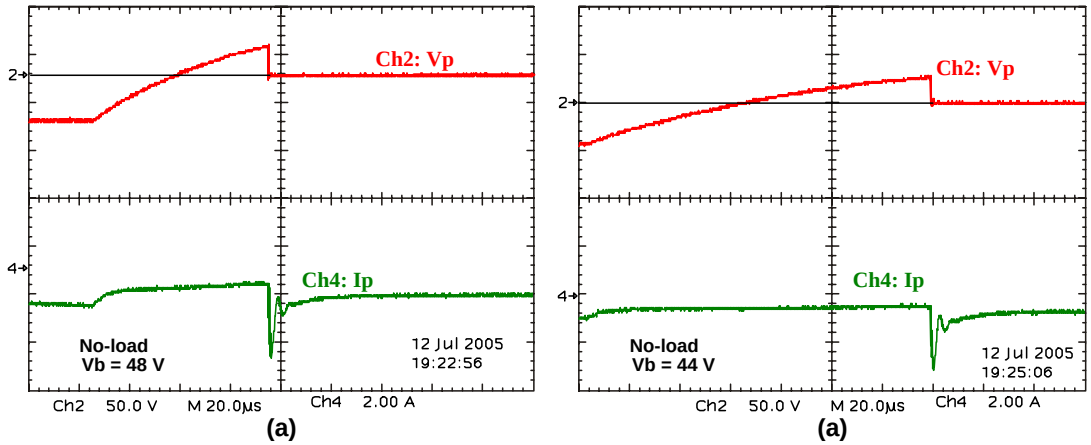


Figure 6.18 - Voltage and Current at the transformer: (a) V_b = 48 V; (b) V_b = 44 V.

The proposed mechanism to control transformer-unbalancing worked properly and showed to be robust. Figure 6.19(a) makes clear the importance of the proposed technique, showing that the transformer saturates even in the presence of a relatively low half wave load if the transformer-unbalancing control is not activated. On the other hand, if the proposed control is activated, perfect balance is achieved, as shown in figure 6.19(b).

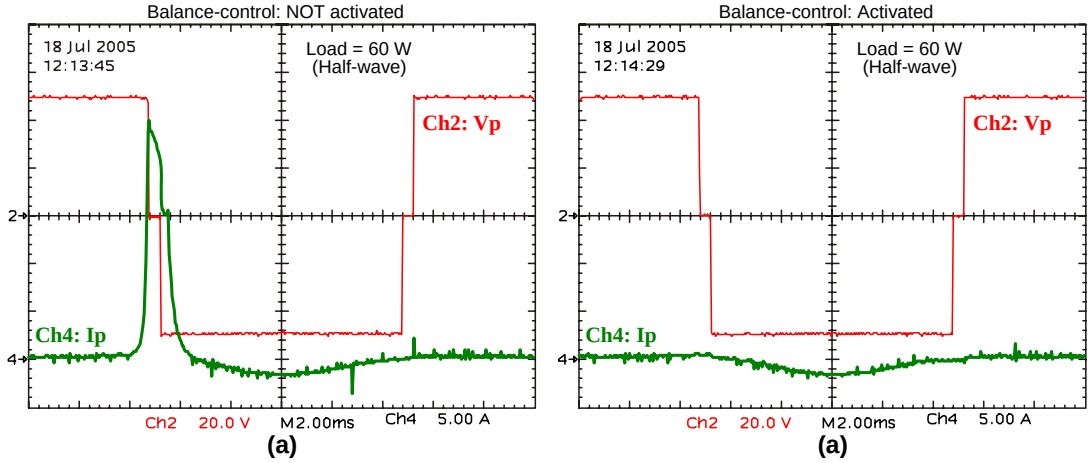


Figure 6.19 - Voltage and current at the transformer:
(a) Without balance-control - 60W half-wave load;
(b) With balance-control - 60W half -wave load

The transformer-unbalancing control mechanism is not only important for the case of unbalanced loads, but it is also fundamental to guarantee smooth converter startup. Figure 6.20(a) and 6.20(b) shows the no-load converter startup without and with transformer-unbalancing control, respectively. Although both startup processes had been smoothed by the gradual increase of the transformer primary voltage, high current peaks were produced when the transformer-unbalancing controller was not activated, as showed in figure 6.20(a). On the other hand, figure 6.20(b) shows that smooth startup is achieved if the transformer-unbalancing controller is activated.

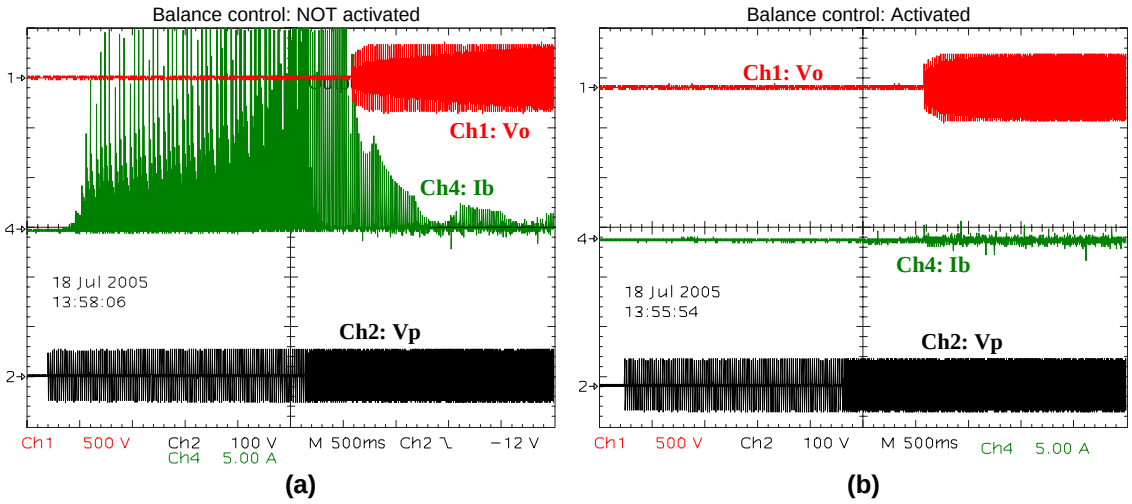


Figure 6.20 - Startup waveforms: (a) without balance-control; (b) with balance-control.

6.4 Resistive, capacitive and inductive load waveforms

The first experiments done to evaluate the prototype made use of near ideal resistive, capacitive and inductive loads. Figures 6.21 and 6.22 show a set of experiments done with resistive loads (prototype feed by a 48 V battery bank). Figure 6.21(a) presents an overall view of both transient and steady state operation of the prototype under a sequence of resistive load steps. As can be seen, despite of the large changes in the input voltage and also in the output current, the converter was capable to produce a stable output voltage.

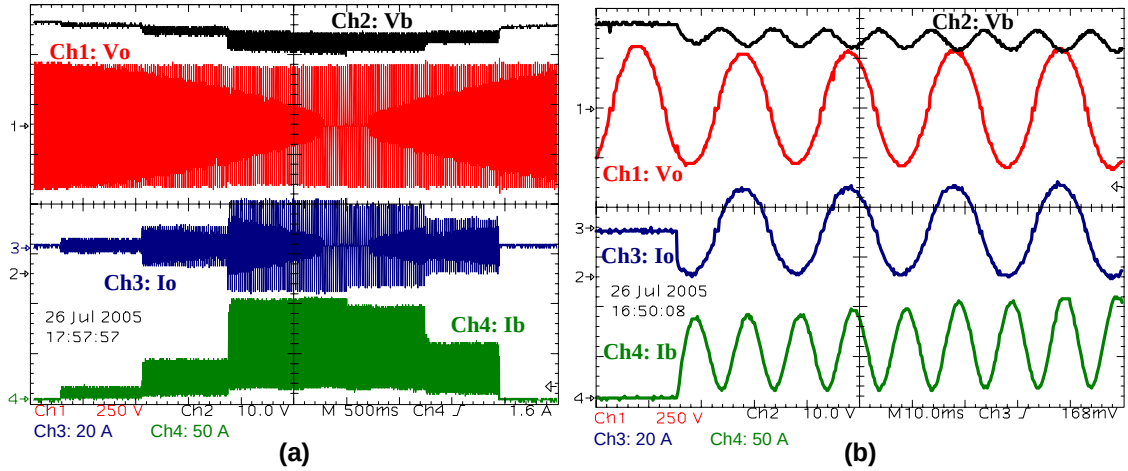


Figure 6.21 - Waveforms for operation under resistive load:
(a) Sequence of load steps.
(b) Single load step of 3.16 kW.

A close view on the insertion transient of a load step of 3.16 kW can be observed in figure 6.21(b), which shows that the transient response has good aspect and no oscillations are presented. However, figure 6.22(a) shows that a quick and deep voltage drop can occur at the turn on instant. This voltage drop can be associated to the output filter inductance, and it may not represent a major problem because its duration is relatively small.

The turn off transient response can be observed in figure 6.22(b). Although fast transient over-voltage peaks are not presented, it is observed an over-voltage condition over some cycles. This over-voltage condition is caused by the low speed dynamics of

the implemented controller firmware. In fact, the design of the controller was not focused on the dynamics response, and further improvement is suggested for future works (no hardware changes are expected, but only changes in firmware).

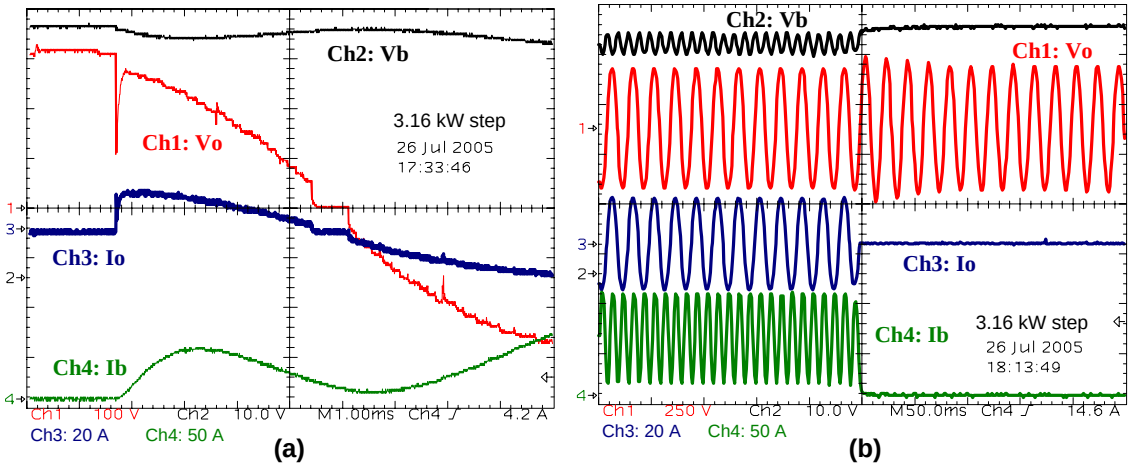


Figure 6.22 - Waveforms for operation under resistive load:
(a) Close-up at the turn-on instant of a 3.16 kW resistive load step;
(b) Turn-off instant of a 3.16 kW resistive load.

Operation of the prototype feeding a nearly pure inductive load is presented in figure 6.23. As showed in figure 6.23(a), the current is delayed by almost 90 degrees and the output voltage did not suffer any perceptible distortion. The bi-directional power flow handling capability of the proposed inverter can be verified in figure 6.23(b), where the input current assumes positive and negative values.

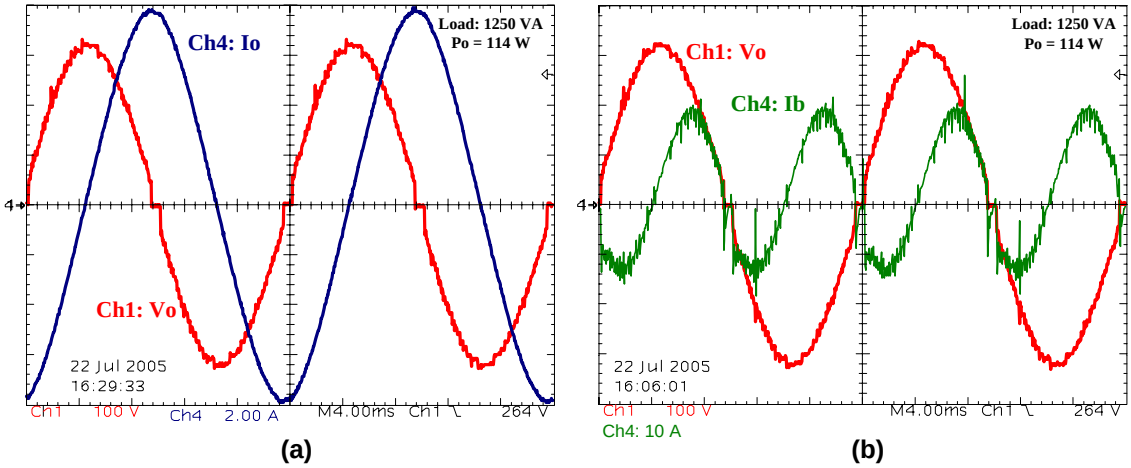


Figure 6.23 - Waveforms for operation under inductive load:
(a) Output voltage and current;
(b) Output voltage and battery current.

The operation of the prototype feeding capacitive loads was not soft as the operation under inductive load. In fact, a strong capacitive load operates as a voltage source that acts as short-circuits at each step transition. Figure 6.24(a) shows the output voltage and current for a 1311 VA / 6 W capacitive load. As can be seen, the output current presents too much distortion while the output voltage is almost free of steps. Also the larger current peaks that appear near the zero crossing of the voltage are due to the presence of large initial voltage steps. Although the current waveform shown in figure 6.24(a) does not appear to be sinusoidal, it presents an advanced phase of 90 degrees, as expected for

a pure capacitive load. Bi-directional power flow can be verified in the current waveform shown figure 6.24(b).

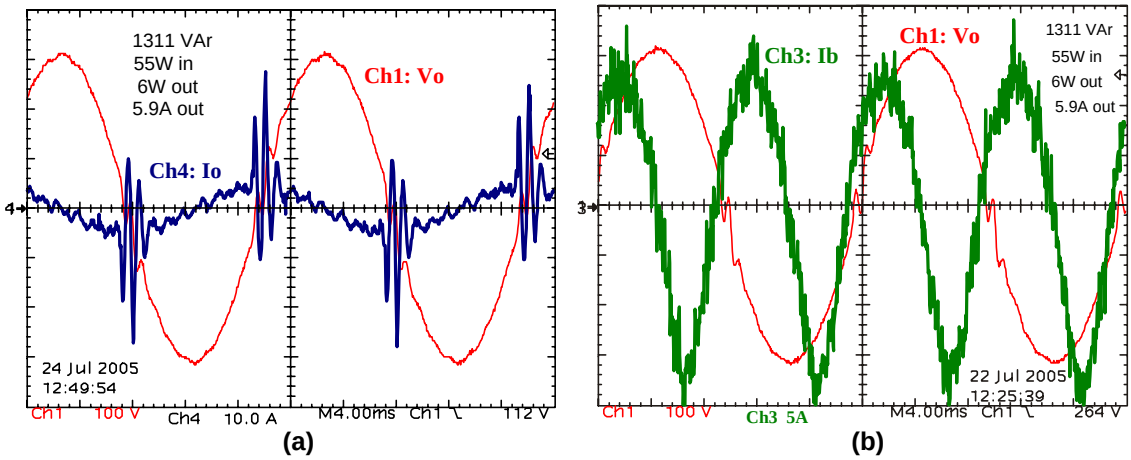


Figure 6.24 - Waveforms for operation under capacitive load:
(a) Output voltage and output current;
(b) Output voltage and battery current.

6.5 Startup of loads

In practice, most loads do not act like pure resistance, inductance or capacitance. Non linear characteristic and high startup currents are usually presented by real loads, such as refrigerators, incandescent and fluorescent lights, single phase motors, computers, and general electronic apparatus. The capability of the proposed inverter to operate such loads is demonstrated in this section.

The refrigerator is commonly desired in residential applications and it is known to be a problem in many small stand-alone systems due to its high startup current. Figure 6.25 shows the waveforms acquired at the startup of a small refrigerator when it is connected to the implemented prototype.

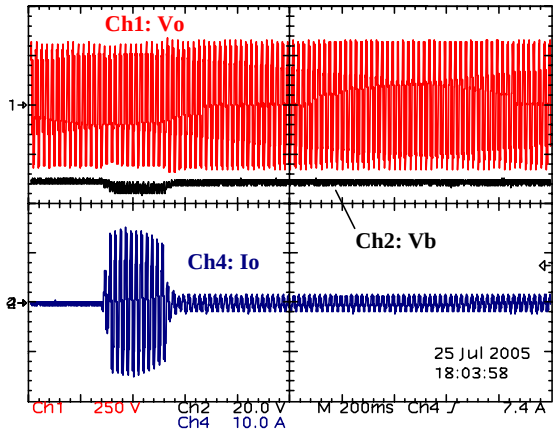


Figure 6.25 - Waveforms at the startup instant of a refrigerator.

At steady state operation, the measured current was 1.0 A (RMS), while according to figure 6.25, the current at startup is approximately 10.6 A (RMS). Thus, even this small refrigerator may require 2.4 kVA at startup. This experiment was repeated several times and the prototype operated without any problem.

Another startup experiment made use of an abrasive wheel machine, and the acquired startup waveforms are presented in figure 6.26. Although the startup transient is longer for this machine, only 3.2 A (RMS) was required. This experiment was also repeated several times and the prototype operated without any problem.

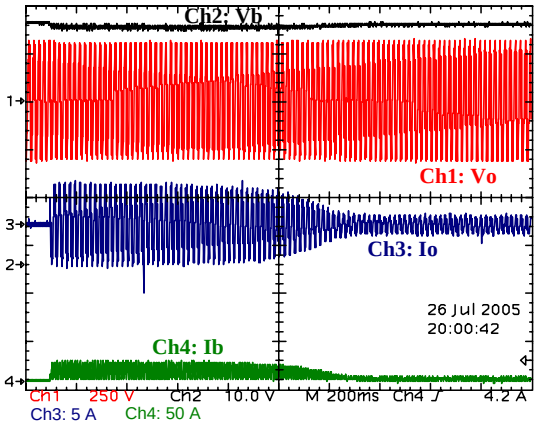


Figure 6.26 - Waveforms at the startup instant of an abrasive wheel machine.

The largest single load that was used to evaluate the implemented prototype was a single phase sawing machine of 2 kW. Figure 6.27 shows the waveforms acquired during its startup. Although this machine includes a kind of soft-start technique (2-step startup), its transient presented current of 22.6 A (RMS) which means an output peak power of approximately 4 kVA (considering the reduced output voltage of 177 V). On the input DC side, the current peak reached approximately 170 A at the input voltage of 44 V, what corresponds to an instantaneous peak power of 7480 W. This experiment was also repeated several times and the prototype operated without any problem.

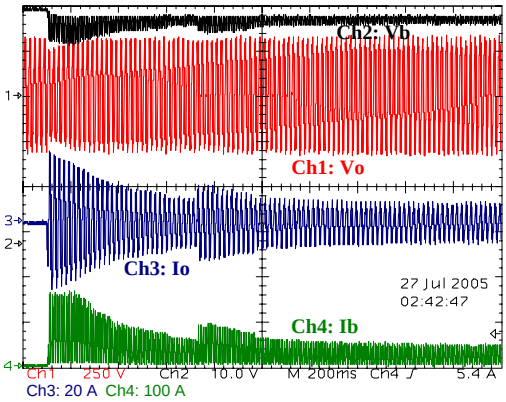


Figure 6.27 - Waveforms at the startup instant of a sawing machine of 2 kW.

A linear power supply is a good example of a non-linear load. In particular, at its startup, it may act like an unbalanced transformer, as shown in figure 6.28. As can be seen, the startup current is strongly non linear and reach a peak of about 20 A_{pk} at the AC side and 100 A_{pk} at the battery side. The prototype worked properly with this load.

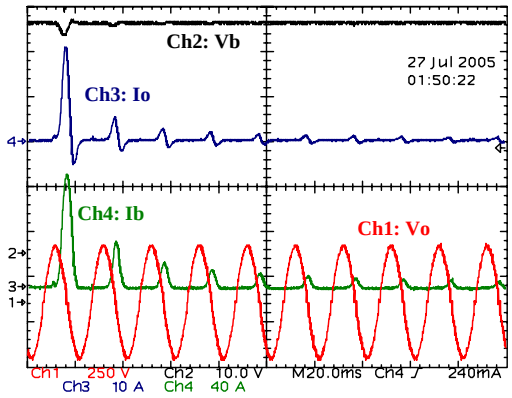


Figure 6.28 - Waveforms at the startup instant of a linear power supply.

In order to reach the operation limit of the implemented prototype, a set of loads had to be connected simultaneously. Figure 6.29(a) shows the startup waveforms for a set of loads composed by: one resistive load of 1 kW, one refrigerator, one single-phase motor and one abrasive wheel machine. As can be seen, the prototype was able to startup all these loads simultaneously.

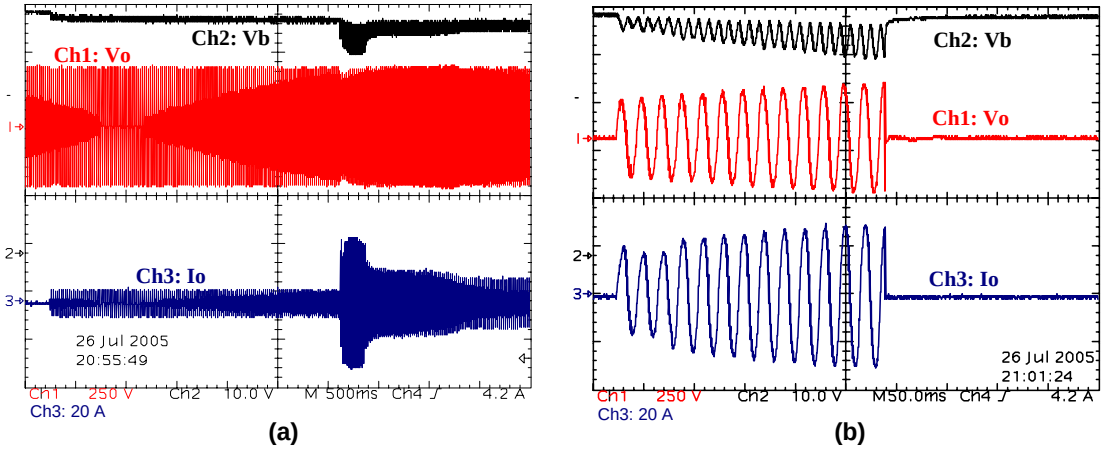


Figure 6.29 - Waveforms at the startup of a group of loads:
(a) 1 kW resistance, refrigerator, motor and abrasive wheel machine.
(b) 2 kW resistance, refrigerator, motor and abrasive wheel machine (failed)

Figure 6.29(b) shows the waveforms acquired when the prototype was experiment with set of loads composed by: one resistive load of 2 kW, one refrigerator, one single-phase motor and one abrasive wheel machine. In this experiment, the loads were already connected to the prototype before it was turned on. However, even with the smooth increase of the output voltage, the input current reached the programmed current limit and the power-stage was turned off by the controller. At the load side, current peak of about 30.0 A at peak voltage of 300.0 V was registered (instantaneous power of 9 kW_{pk}). In terms of RMS values, current reached the peak value of 21.2 A at the voltage of 212.1 V (surge power of power of 4.5 kW).

In order to demonstrate that the stepped output waveform of the proposed inverter is not a problem for sensible electronic devices, a personal microcomputer was connected to the prototype. Figure 6.30 shows the steady state waveforms, where it is possible to see the non linear characteristic of the microcomputer power supply. The microcomputer operated normally during this experiment. The noise presented in the output current can be attributed to the output-stage switching (in this case, the load current is so small that the noise assumes similar magnitude).

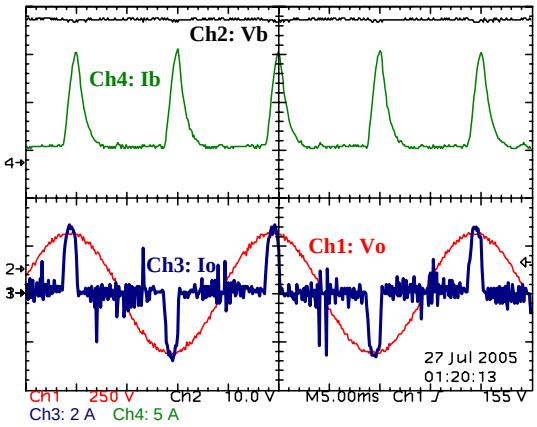


Figure 6.30 - Waveforms for operation with a microcomputer.

6.6 Battery-charge-mode using Sunny Boys

The proposed converter is bi-directional and this feature can be used to charge the battery bank if its output is connected to a power source with current source characteristic. This type of operation was realized by using solar panels and grid inverters, using the configuration shown in figure 6.31. The prototype was connected to 2 Sunny Boys grid inverters fabricated by SMA. Each Sunny Boy was feed by a 900 W_{pk} solar panels arrays (total of twenty four 75 W_{pk} PV modules, organized in two arrays of 12 modules). The DC side of the inverter was connected to a 48 V battery bank.

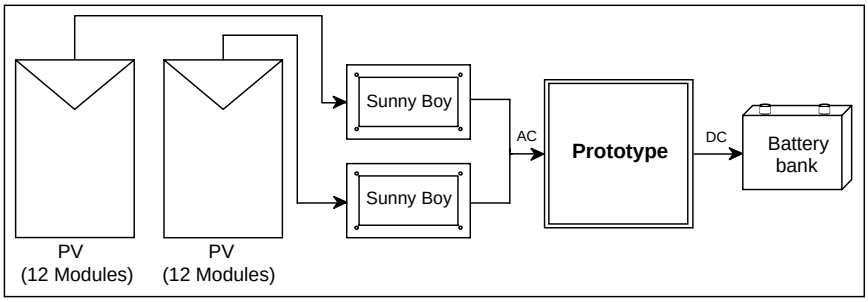


Figure 6.31 - Block diagram of the battery-charge-mode experiment.

Figure 6.32(left) shows the panel array modules while figure 6.32(right) shows the prototype and Sunny Boys (at the back).

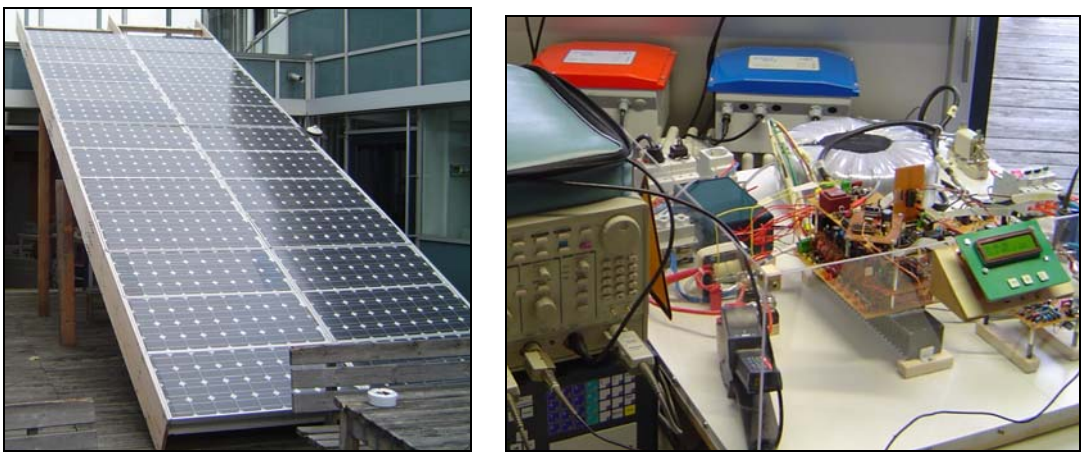


Figure 6.32 - Pictures of the battery-charge-mode experiment setup.

The acquired waveforms are shown in figure 6.33. As can be seen, the battery current oscillates with 100 Hz and assumes only negative values, thus charging the battery bank. The AC current flowing into the prototype is opposite to the AC voltage, showing that the power flows into the converter. Some disturbances can be found near the zero crossing and can be associated to the hold-on-at-zero interval and also to the large initial voltage steps presented in the multilevel waveform.

It is important to note that the Sunny Boys periodically test the grid (in this case, the AC side of the prototype) by verifying its impedance, in order to shutdown its operation in case of grid disconnection. This means that the prototype could act like a real grid from the point of view of the Sunny Boys.

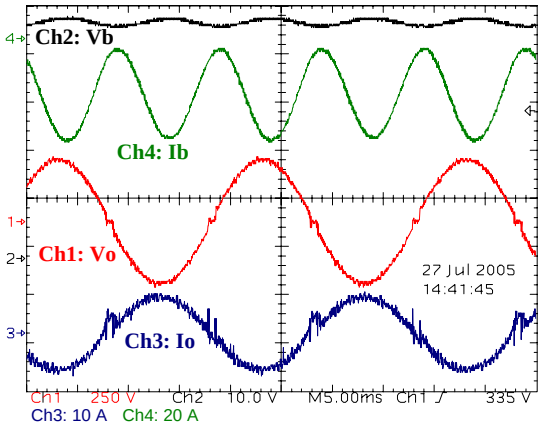


Figure 6.33 - Waveforms for operation in battery-charge-mode.

6.7 Characteristic curves

6.7.1 No-load consumption

Figure 6.34(a) shows the no-load consumption as a function of the input voltage. As can be seen, the input voltage has great influence in the no-load consumption and its characteristic looks like an exponential curve. This fast increase can be associated with the increase of the transformer no-load losses as its primary voltage is increased.

The standby characteristic of the prototype is showed in figure 6.34(b). At this operation mode, only the auxiliary power supply and controller are operating and no output voltage is produced. As can be seen, this characteristic curve is approximately linear, although it does not change significantly over all input voltage range.

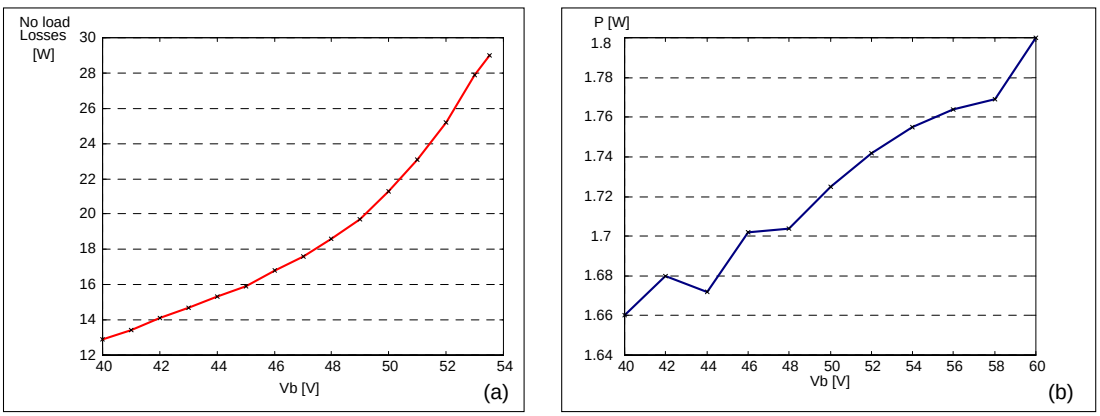


Figure 6.34 - (a) No-load consumption versus input voltage;
(b) Stand-by consumption versus input voltage.

Another parameter that influences the no-load consumption is the number of output levels used to produce the output voltage, as shown in figure 6.35. In fact, loss increase can be associated to more switching activity and also to the higher output voltage. As can be seen, loss increase of approximately 1.75 W occurs when number of levels is increased from 16 to 30.

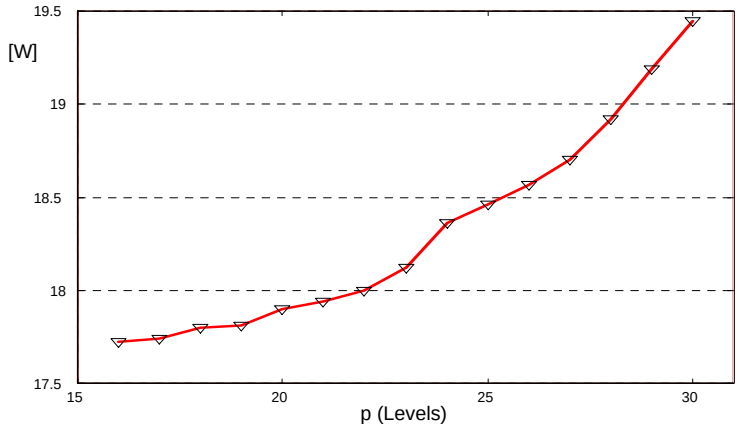


Figure 6.35 - No-load consumption versus p.

The no-load losses are attributed to many components and figure 6.36 shows how losses are distributed along the prototype when the input voltage is 48 V. As can be seen, the transformer consumes 10.6 W and is responsible for 57% of the total no-load losses, followed by the output-stage switching activity (2.8 W or 15%). This diagram can help future design optimization.

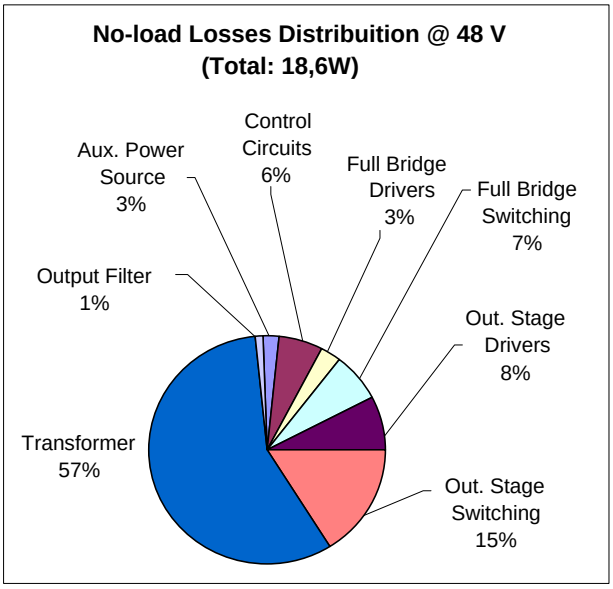


Figure 6.36 - No-load consumption distribution for input voltage of 48 V.

6.7.2 Efficiency characteristic

In this section the efficiency characteristic of the proposed converter is investigated according to the variation of input voltage, output voltage, temperature and type of load.

Because the operation frequency is low, losses are mainly attributed to conduction losses in cables, protection devices, connections, switches and transformer. Figure 6.37 shows the conduction resistance of all devices between the input terminals and H-bridge input. Total resistance in this path is 2.89 mΩ what corresponds to approximately 40 % of the transformer primary resistance, showing that the design of wiring and protection have significant influence on the efficiency when the converter operates with heavy loads.

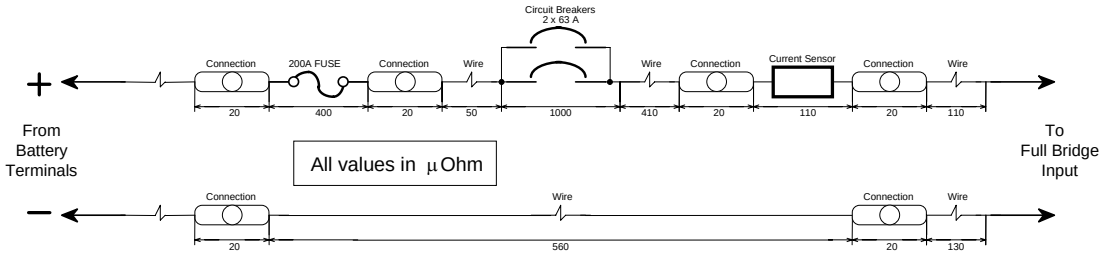


Figure 6.37 - Resistance of all input elements (diagram).

The complete efficiency versus output power characteristic curves of the prototype is shown in figure 6.38, while figure 6.39 presents only the range starting at 250 W.

Peak efficiency of 96.0 % at an output power of 945 W was measured for an input voltage of 48 V. Some discontinuities presented in the curves can be associated to scale changes of the measurement instrument or to changes in the number of levels used to produce the output voltage waveform.

Considering the 48 V curve as a reference, it is possible to conclude that lower input voltages improve the converter efficiency at light loads (due to the lower no-load losses). On the other hand, because the input current is higher at a lower voltage, the converter efficiency for heavy loads decreases as the input voltage decreases. The opposite effect occurs if the input voltage increases, what makes efficiency lower at light loads and higher for heavy loads.

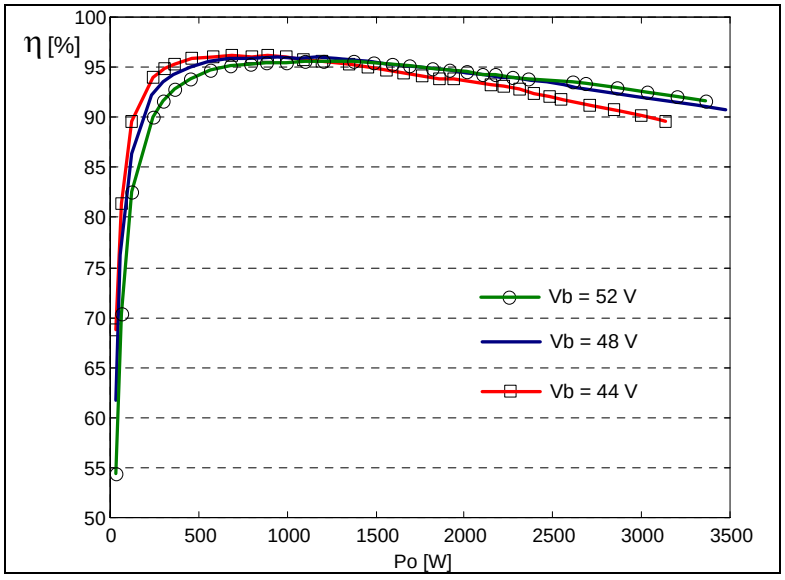


Figure 6.38 - Efficiency x output power characteristic (resistive load).

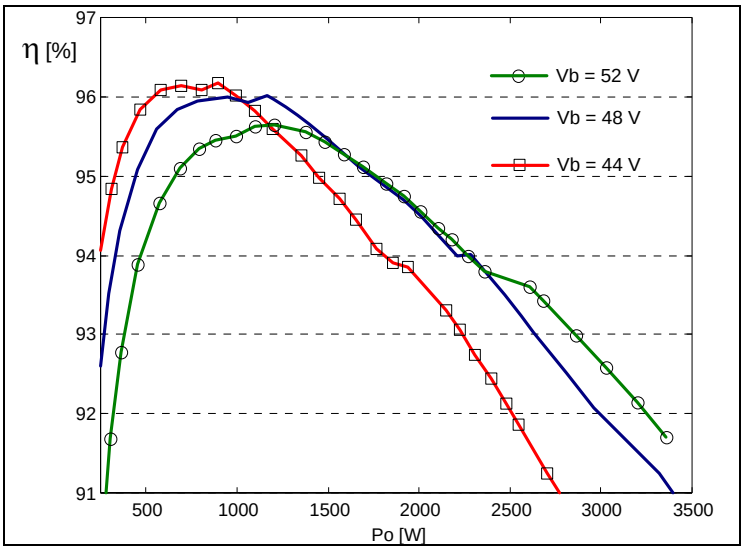


Figure 6.39 - Efficiency x power characteristic (resistive load: 250 W - 3500 W).

The half-wave load used to evaluate the prototype was composed by a diode in series with resistive loads, as shown in the detail inside figure 6.40. For an input voltage of 48 V, the efficiency versus output power characteristic is shown in figure 6.40. Comparing this curve with the curve shown in figure 6.38, it is possible to conclude that, for the same output power, the efficiency for half-wave load is lower then for a normal resistive load. In fact, for the same output power, the RMS current at any point of the inverter is higher in the case o a half wave load, what increases the conduction losses. The value of 1500 W was the highest value supported by the prototype.

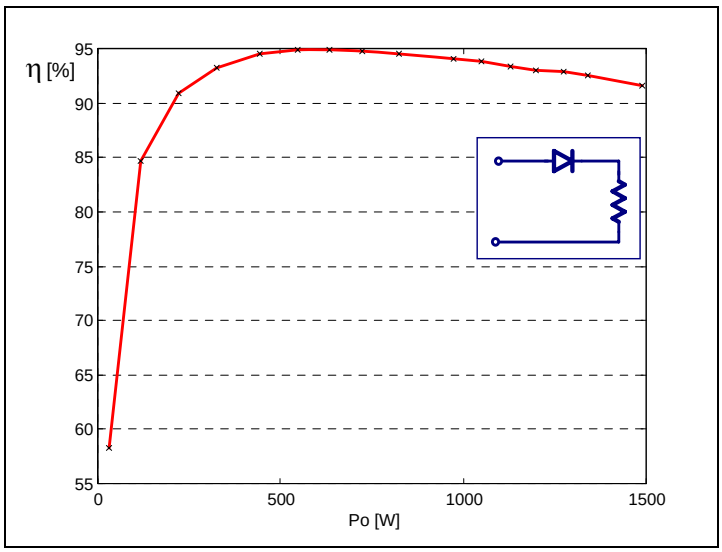


Figure 6.40 - Efficiency x power for operation with half-wave load.

The output voltage value also affects the efficiency characteristic, as shown in figure 6.41. This experiment was done by varying the number of levels used to compose the output waveform, while the input voltage was fixed to 48 V and the load was fixed to the value of 1 kW (resistive load). As can be seen, the efficiency increases with the increase of the output voltage. This can be justified by the decrease of the output current and the consequent decrease of the conduction losses.

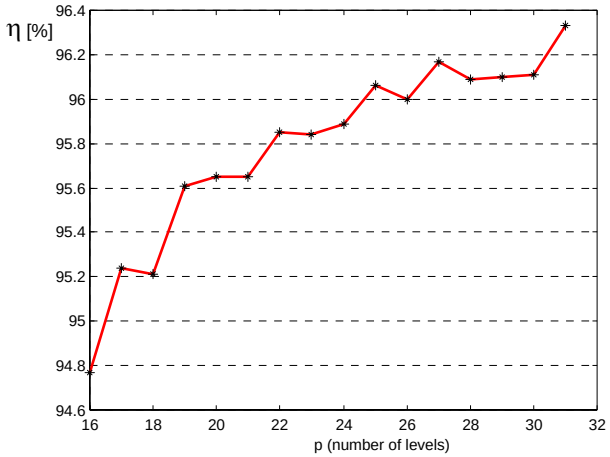


Figure 6.41 - Efficiency versus p (resistive load of 1 kW).

Experiments with variable capacitive and inductive loads were done in order to determine how the load power factor influences the converter efficiency. For constant apparent output power of 1 kVA and 2 kVA, the power factor of the load was varied and the curves shown in figure 6.42 were traced. Peak efficiency is obtained for unitary power factor and lower efficiency is found for any non-unitary power factor. This effect is justified by the additional conduction losses due to the circulation of the reactive current component. It is interesting to note that, for a same power factor value, the capacitive load present lower efficiency than the inductive load. In principle, capacitive loads produce additional losses due to the presence of high current peaks, as was showed in figure 6.24.

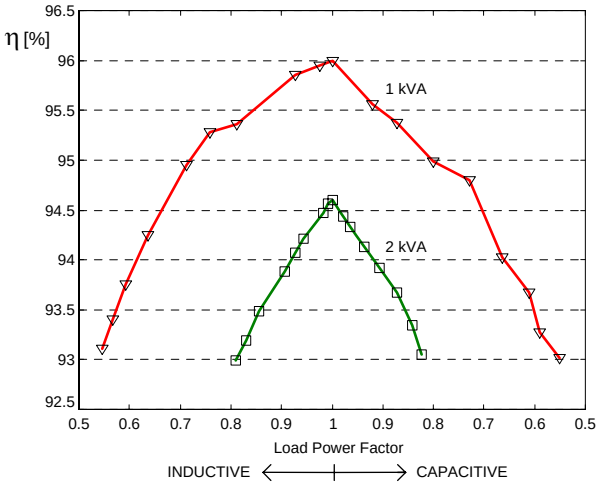


Figure 6.42 - Efficiency versus power factor.

Figure 6.43 shows the efficiency curves for the battery-charge-mode operating with battery voltages of 48, 50 and 52 V. This experiment was not easily done because the sun radiation was very inconstant (due to clouds) and also because the battery voltage had to be controlled by adding a DC load. This is why the curves presented in figure 6.43 have different number of points which are unequally spaced. As can be seen, peak efficiency of about 96% at battery voltage of 48 Volts was achieved, showing that the performance of the converter operating at this mode is quite similar to the operation in inverter mode. The influence of the battery voltage is evident, and efficiency decrease with voltage increase can be mainly associated to the increase in the transformer no-load losses.

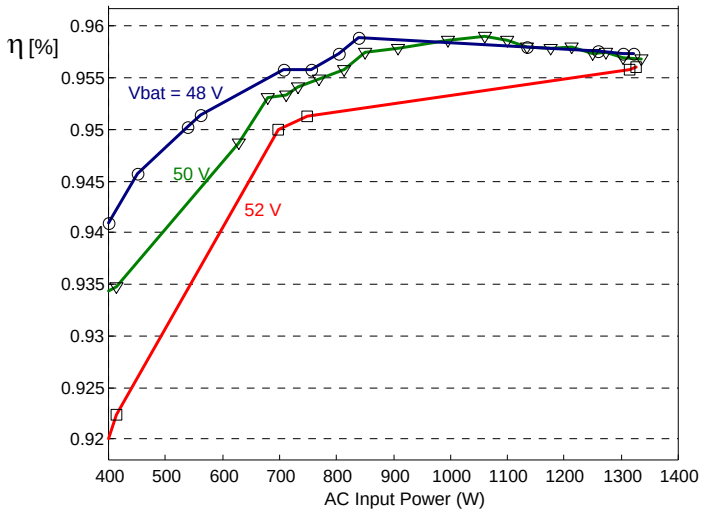


Figure 6.43 - Efficiency characteristic for battery-charge-mode.

It is interesting to observe that the efficiency characteristic is affected by the temperature of the diverse components. In fact, temperature rise increases conduction resistances of wires and MOSFETs, thus increasing conduction losses.

For an input voltage of 48 V and an arbitrary constant output power of 2250 W, the achieved efficiency versus time characteristic is shown in figure 6.44(a). As can be seen, an efficiency drop of about 0.5 % occurred in consequence of the temperature rise.

This experiment was done at an approximately constant room temperature of 24 °C and the evolution of the temperature at the external surface of the output-stage heat-sink, H-bridge heat-sink and transformer are shown in figure 6.44(b). No forced ventilation in heat-sinks was used but the prototype was an opened device. After more then 4 hours, the transformer temperature did not converged, but the heat-sink temperature converged to approximately 45 °C and 57 °C for the H-bridge and output-stage, respectively.

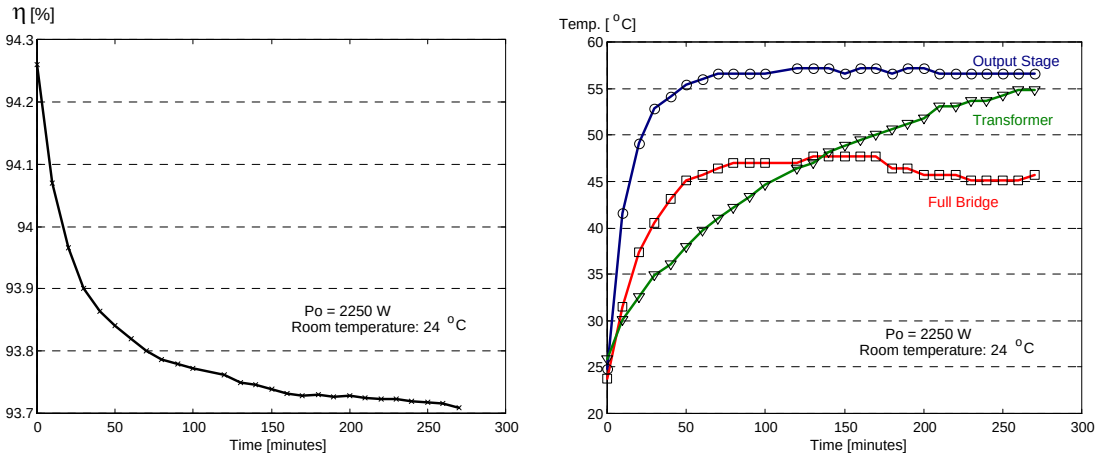


Figure 6.44 - (a) Efficiency versus time. (b) Temperature versus time.

6.8 Non-conventional experiments

The maximum allowed THD of 5% has imposed a limit to the hold-on-at-zero interval so all presented experiments were done with a fixed value of 0.7 ms. However, if the hold-on-at-zero interval is increased, then it is possible to reduce de no-load consumption and consequently increase efficiency at light loads. On the other hand, the output waveform can become strongly distorted and the THD may be higher then 5%.

Figure 6.45(a) shows both variations of no-load consumption and output voltage THD as a function of the hold-on-at-zero interval (input voltage of 48 V). As can be seen, if the hold-on-at-zero interval is increased from 0.7 ms to 3 ms then the no-load consumption is reduced from 18.6W to 14.1W while the THD is increased from 3% to 26%. The reduction in the no-load losses implies in efficiency increase, as shown in figure 6.45(b). In fact, peak efficiency of about 96.4% is reached by using a hold-on-at-zero interval of 3 ms.

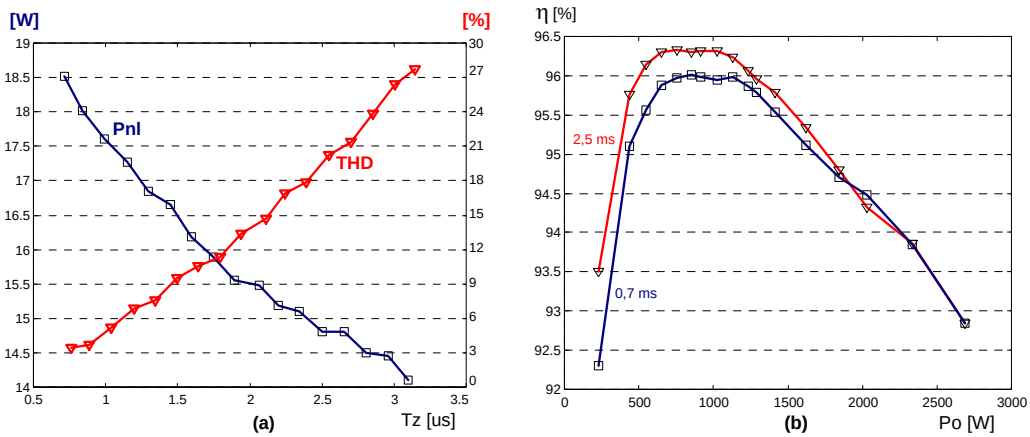


Figure 6.45 - (a) No-load consumption and THD versus hold-on-at-zero interval;
(b) Efficiency characteristic for hold-on-at-zero of 0.7 ms and 2.5 ms.

In particular, for loads that present an input based on a rectifier and filter capacitor, the distortion produced by bigger hold-on-at-zero interval may not alter significantly their operation. Figure 6.46(a) and 6.46(b) demonstrates a good example of such situation, where a linear power supply is fed by the prototype operating with hold-on-at-zero intervals of 0.7 ms and 3 ms, respectively. As can be seen, the load current, and also the battery current, remains almost the same for both cases, but converter efficiency was increased from 88.9% to 92.3% in consequence of the hold-on-at-zero interval increase.

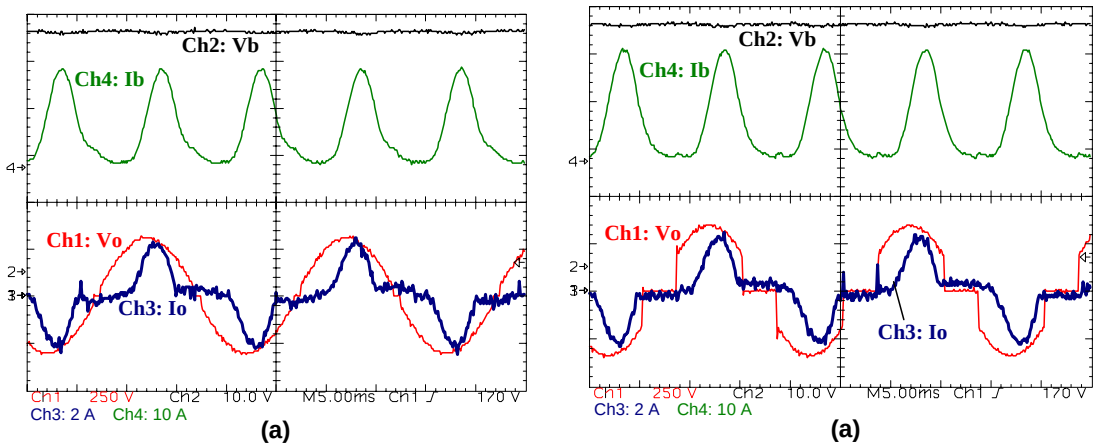


Figure 6.46 - Waveforms for operation with a linear power supply:
(a) Hold-on-at-zero of 0.7 ms; (b) Hold-on-at-zero of 3.2 ms.

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7 Final Analysis

7.1 Comparison with other inverters

A summary of the main characteristics of the implemented prototype and some commercial inverters is shown in table 7.1.

Table 7.1 - Specification data of some commercial converters and implemented prototype.

No	Inverter	Vin [V_{DC}]	Vout [V_{RMS}]	Power [VA]	η_{pk} [%]	No-Load [W]	Surge Power	Surge Current	Weight [kg]
1	Implemented prototype	48	230	3000	96.0	18.6	1.5x	1.5x	-
2	Phoenix 48/3000/35	48	230	3000	95.0	10.0	2x	-	18
3	Studer C3548	48	230	3500	95.0	12.0	3x	-	30
4	Dakar 48/3000/50	48	230	3000	90.0	4.8	2x	-	36
5	SMA Sunny Island 3324	24	230	3300	94.5	22	1.5x	3.5x	39
6	SMA Sunny Island	60	230	3300	92.0	<10	2x	-	45
7	Trace SW3048	48	230	3300	95.0	16.0	-	2.3x	48
8	Xantrex SW2548	48	120	2500	95.0	<20	-	3.8x	52

All commercial inverters data were obtained from the respective manufacturer manuals and they present nominal power around 3000 VA [44-50]. As can be seen, the implemented prototype presents the best peak efficiency (96 %).

Regarding no-load consumption, the proposed inverter present a reasonable value if it is considered that it competes with only inverters 2, 3 and 7. In fact, inverters 4 and 6 can not be used as reference because their poor efficiency characteristic, and inverters 5 and 8 probably present higher no-load consumption allied to worst efficiency. Moreover, the no-load consumption should not be analyzed as an isolated parameter, because its influence in the overall energy conversion efficiency must consider a load profile. Taking this into account and considering the typical load profile presented in section 2.1, conclusive investigation can be done by observing figure 7.1. It should be noted that the following analysis do not consider inverter 3 because its efficiency characteristic was not available.

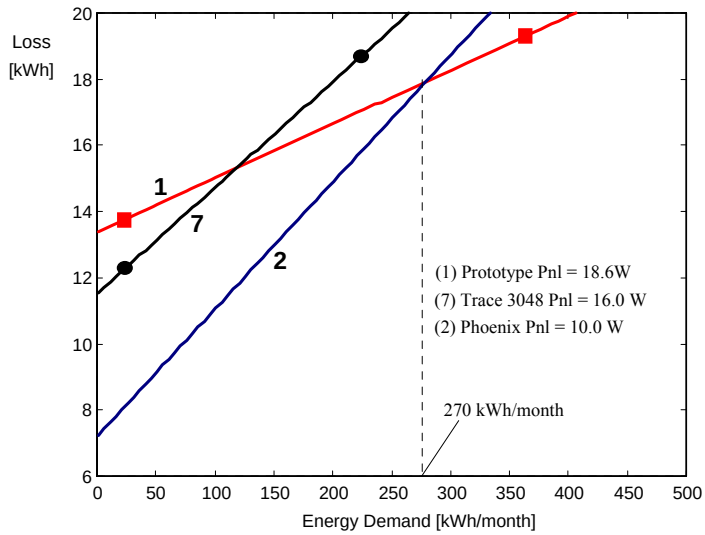

Figure 7.1 - Monthly energy loss versus energy demand for the implemented prototype and also for the selected commercial inverters.

Figure 7.1 shows that the relatively higher no-load loss of the proposed inverter is compensated by its high conversion efficiency as the energy demand is increased. In terms of numbers, the proposed inverter presents the best overall efficiency for any energy demand above 270 kWh /month. In fact, the relatively high no-load consumption can be mainly attributed to the current employed multi-winding transformer, which can be further improved, as discussed in section 7.3.

Regarding surge power capability, maximum input current was limited for safety reasons during the experiments done in this work. Nevertheless, according to the switches specification, surge power can reach more than 2.5 times the rated current.

7.2 Economical viability

Table 7.2 shows the average price of some commercial inverters that were obtained thought internet from diverse worldwide sellers.

Table 7.2 - Prices of selected commercial inverters.

Inverter	Power	Mean Price [€]*	€/W
Phoenix 48/3000/35	3000	2.800	0.93
Studer C3548	3500	1.800	0.51
Xantrex SW2548	2500	1.800	0.72
SMA Sunny Island 3324	3300	2.300	0.70
		Average ==>	**0.72**

* prices from internet, search date: 25/03/2006.

The achieved average value of 0.72 €/W is in accordance with the value announced by the website "solarbuzz.com", that is equal to 0.69 €/W in march of 2006 [99]. Thus, price of an inverter of 3000 VA is expected to be around € 2100.00.

In order to have an idea of the expected economical viability of the proposed inverter, rough cost estimation of the main components (power structure) of the implemented prototype and two other converter topologies are given in tables 7.3, 7.4 and 7.5. It is important to note that cost of other components, such as protections, controller, instrumentation and case, was not taken into account because it was supposed that all topologies require these components and their cost are more influenced by the inverter design than by the topology. The present analysis intends to calculate relative cost difference (not absolute cost) and its respective percentage in relation to a reference price.

Table 7.3 - Prototype: cost of main components (power structure).

Component	Qty.	Unit Price [€]	[€]
Multi-winding transformer	01	150	150.0
HCPL-3205 (isolated MOSFET drive)	14	1.2	16.80
IRFP2907	8	3.3	26.40
IRF3205	8	0.7	5.60
IRF2807	4	0.7	2.80
IRFP260N	4	1.40	5.60
APT30M40LVR	4	12.0	48.00
Diverse (snubber components)	28	0.70	19.60
Diverse (isolated drive power supply)	10	1.5	15.00
Diverse (additional circuit board space)	10	1.0	10.00
Output filter	1	10	10.00
		Total ==>	**309.8**

Average prices (1k units) from internet, or estimated: search date: 25/03/2006 [D1-D9].

Table 7.4 - Multiple-transformer/3 (3 kVA): cost of main components (power structure).

Component	Qty.	Unit Price [€]	[€]
Power transformer (9/13 of total power)	01	110	110.0
Power transformer (3/13 of total power)	01	40	40.0
Power transformer (1/13 of total power)	01	20	20.0
IRF2110 (MOSFET driver)	6	2.3	13.80
IRFP2907	4	3.3	13.20
IRF3808	4	1.9	7.60
IRF2807	4	0.7	2.80
Diverse (snubber components)	12	0.70	8.40
		Total ==>	**215.80**

Average prices (1k units) from internet, or estimated: search date: 25/03/2006 [D1-D9].

Table 7.5 - HF-PWM inverter (3 kVA / 20kHz): cost of main components (power structure).

Component	Qty.	Unit Price [€]	[€]
IRFP2907 (MOSFET/input H-bridge)	8	3.3	26.40
IRG4PC50W (IGBT/output H-bridge)	8	2.6	20.80
Diode MUR3060	4	1.1	4.40
Electrolytic capacitor 470uf x 400V	1	5.0	5.00
HF transformers (ferrite, core EE 65/27)	5	12.0	60.0
IRF2110 (half-bridge driver)	2	2.3	4.60
Isolated high-speed IGBT driver module	4	8.0	32.00
Diverse (snubber components)	16	0.70	11.2
Input filter (High-frequency)	1	10.0	10.00
Output filter	1	10.0	10.00
		Total ==>	**184.4**

Average prices (1k units) from internet, or estimated: search date: 25/03/2006 [D1-D9].

Considering the multiple-transformer/3 topology as the reference and the estimated inverter price of €2100.00, then the proposed inverter present approximately 4.5 % (or +€ 94.00) higher cost, and the HF-PWM inverter 1.5 % lower cost (or - €31.40).

It is also interesting to note that the proposed inverter makes possible to achieve better resolution with relatively low increase in cost. Table 7.6 shows that the addition of an output cell (low voltage) corresponds to €18.00 increase in material cost.

Table 7.6 - Additional cost per output-cell.

Component	Qty.	Unit Price [€]	[€]
Additional transformer winding	01	5.0	5.0
HCPL-3205 (isolated MOSFET drive)	02	1.2	2.4
Diverse (snubber components)	4	0.70	2.8
Diverse (isolated drive power supply)	2	1.5	3.0
Diverse (additional circuit board space)	2	1.0	2.0
Low voltage MOSFET	4	0.7	2.8
		Total ==>	**18.0**

* prices from internet, search date: 25/03/2006 [D1-D9].

7.3 Inverter improvement

Further inverter no-load reduction can be mainly achieved by modifying the multiple-winding transformer design. The simplest way to reduce the transformer no-load consumption is to increase the number of turns in its primary. In this case, if a same core is used, then coil wire area must be decreased in order to fit the same window area. In consequence, coil resistance of both primary and secondary are increased by the

square of the voltage change factor, and the same occurs with the losses due to winding resistances.

The relation between no-load consumption and coil resistances can be estimated through the transformer no-load power versus input voltage characteristic, and considering that the transformer wiring losses can be modeled by a single equivalent primary resistance (R_{eq}), then it is possible to determine the R_{eq} versus no-load characteristic, as shown in figure 7.2. Finally, the R_{eq} x P_{nl} characteristic can be used to calculate the weighted conversion efficiency versus no-load characteristic, also shown in figure 7.2 (see the calculation sheet shown in appendix G).

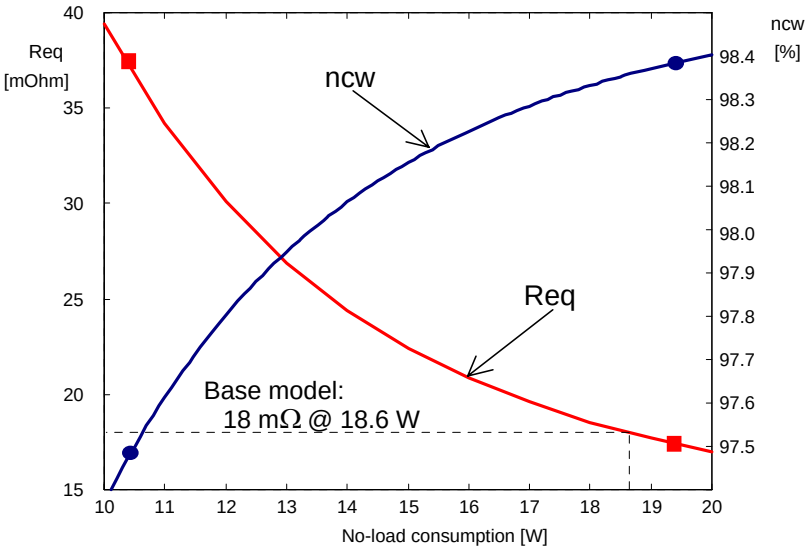

Figure 7.2 - Conversion efficiency and equivalent resistance versus no-load consumption.

As can be seen, reduction of no-load consumption implies in lower conversion efficiency. In practice, for a given value of energy demand, it is possible to determine an optimum no-load consumption that corresponds to a minimum value of energy loss. Figure 7.3 illustrates how this process takes place.

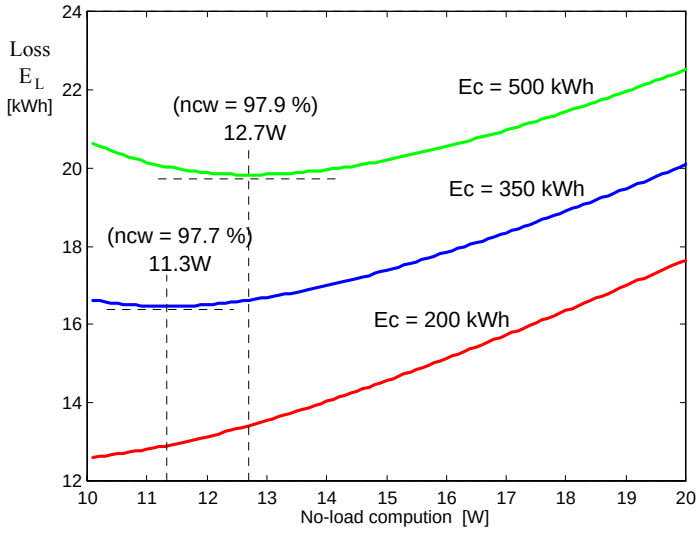

Figure 7.3 - Monthly energy loss versus no-load consumption for demands of 200, 350 and 500 kWh/month.

For example, for a 500 kWh/month demand, the inverter will present the lowest losses if the transformer is designed to save 5.9 W (18.6 W - 12.7 W) at no-load. Nevertheless, if the no-load consumption is made lower than this value, then consequent decrease of the conversion efficiency will produce more loss than the savings due no-load reduction.

The influence of different transformer design can also be observed in the inverter efficiency characteristic curves shown in figure 7.4.

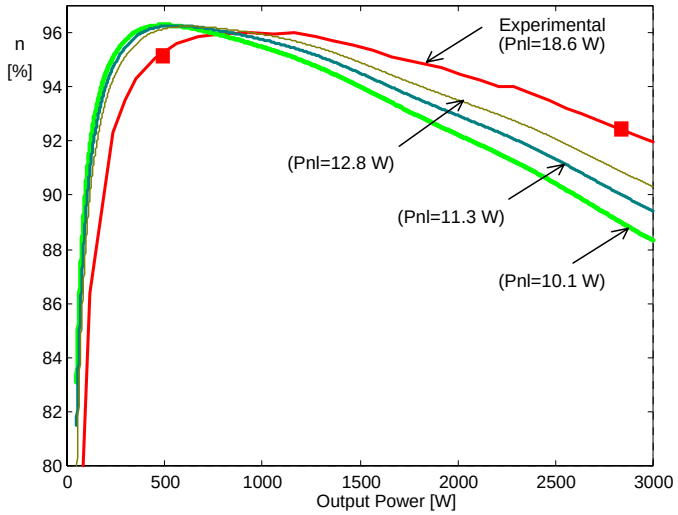

Figure 7.4 - Efficiency characteristic for different transformer designs.

Figure 7.4 shows that the transformer unit used in the prototype is not optimized for the low power region. Also, it can be observed that inverter efficiency can reach a peak value of about 96.3% with a new transformer design (with the cost of full-load efficiency decrease). Also, in comparison with other inverters, use of an optimized transformer can make the proposed inverter present the best overall efficiency for any practical value of load demand, as shown in figure 7.5.

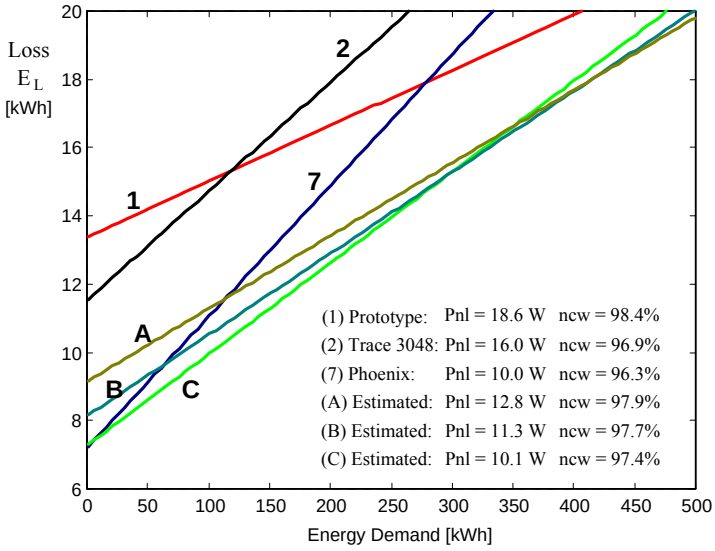

Figure 7.5 - Monthly energy loss versus demand for the implemented prototype (1), selected commercial inverters (2,7) and prototype with new transformer designs (A,B,C).

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8 Conclusions

8.1 Conclusions

This dissertation had investigated a high efficiency multilevel inverter topology which has great potential for application in stand-alone renewable energy systems. The presented study was focused on small systems (< 10 kW_p) and it was showed that most typical system configurations store energy in battery banks in order to overcome the intermittence and peak power limitation of renewable energy sources. In this context, it was also identified that these systems require inverters with improved characteristics of reliability, capability to start heavy loads, efficiency and robustness. In fact, all these benefits can be achieved through the use of multilevel topologies.

Although several multilevel topologies have been successfully employed in industrial and power systems applications, it has been showed that only few topologies are suitable to implement inverters for small stand-alone systems, where usually only one single DC voltage source is available and the load is not precisely defined. According to these requisites and considering only the topologies based on low-frequency switching, it was found that the multiple-transformer and multi-winding-transformer topologies are the most efficient; the latter is the topology adopted in this work.

In both multiple-transformer and multi-winding-transformer topologies, major losses are associated to conduction losses in the switches and transformer losses. Knowing that transformer conduction losses are more representative than conduction losses in current available semiconductor switches, it can be concluded that the adopted topology can achieve the best feasible efficiency characteristic because the load current is shared among transformer coils and shunt switches.

The use of low-frequency switching (< 3 kHz) implies in negligible switching losses and consequently high efficiency. In addition, low-frequency operation allows the use of rugged snubbers that limit dv/dt variations without inserting appreciable losses. Considering that temperature rise and voltage stress are the main factors that decrease semiconductors lifetime, then it is expected that higher efficiency and individual switch protections can contribute to increase inverter reliability. Also, individual snubbers can be very effective against unpredicted fault conditions which can lead to inverter failure.

Apparently, the line-frequency transformer and relatively high number of components employed in the adopted topology appear to be serious drawbacks. However, additional weight and volume required by the transformer is not a problem for most systems, once these inverters normally remain in the same place after their installation. Also, it is well known that amount of components does not imply necessarily in reliability decrease and the use of more switches can be even a benefit if it is considered that power dissipation are distributed among them.

The adopted topology was investigated in detail and the presented results are useful for future designs. It was found that acceptable THD (< 5%) and voltage regulation (+ 5 %, -10%) can be guarantied in practice by structures with at least 4 output cells. Related to the transformer specification, it should be noted that its rated power must be higher than the inverter's rated power (about 30% higher) because the particular voltage and current relations required by the adopted topology. It is also showed that optimum transformer design must consider that the load profile of typical stand-alone systems is concentrated around a small fraction of its rated power.

A new method to identify and correct unbalanced load condition was developed specifically to the proposed inverter. It allows the inverter to operate even with pure half-wave loads and also guarantees smooth inverter startup. The introduced self-control mechanism, which makes use of the H-bridge snubbers, implements an automatic fine balancing of the transformer magnetization current. Although the hold-on-at-zero intervals introduced by the balance-control method distort the output voltage waveform (THD is increased in about 2 %), it contributes to decrease the transformer magnetization current and no-load losses.

Ideally, each output-stage switch should be controlled independently and in accordance with the output voltage polarity and load current direction. However, in order to simplify the implemented circuits and to reduce cost, a simplified control was adopted, in which both switches that compose a bi-directional switch are controlled by the same signal. In consequence, the output-stage switch snubbers can be submitted to the full load current during dead-time periods. In this case, special attention must be given to the design of the output-stage in order to avoid voltage stress across the switches and over-current thought the snubber zenner diodes.

A 63-level (5-cell output-stage) / 3 kVA prototype was implemented to validate the proposed inverter. Experiments with adjustable resistive, inductive and capacitive laboratory loads were done to trace the prototype characteristic curves, and several standard appliances, varying from computers to heavy duty sawing machines, worked properly when supplied by the proposed inverter. The prototype was capable to feed experimental half-wave loads up to 1.5 kVA without any problem. Bi-directional power flow capability was demonstrated though the operation of highly inductive and capacitive loads and battery-charge-mode was validated by connecting grid-interactive converters directly to the inverter output.

Peak efficiency of 96.0% and no-load consumption of 18.6 W were measured at rated input voltage (48 V). As expected, good quality waveform was achieved, presenting THD of less than 4% and static output voltage regulation within + 5%, -6%. Maximum measured surge power capability was 4.500 W (1.5 times the rated power), which was limited by the inverter protections. However, according to the prototype design, it is expected that surge power up to 2.5 times the rated power can be achieved.

Considering a typical load profile and in comparison with high-quality commercial inverters of similar power and voltage ratings, it was found that the implemented prototype can achieve the best efficiency performance for any load demand greater than 270 kWh/month. Moreover, through solely modifications in the design of the multi-winding transformer, it was demonstrated that it is possible to achieve peak efficiency of 96.3% and superior performance for any practical load demand.

In fact, it is expected that the proposed inverter can reach very high efficiency (> 98%) as a cost of higher price and volume. This is possible because switching losses are negligible and conduction losses can be decreased as much as desired by using better and/or oversized components.

Regarding cost, slightly high cost is associated to the proposed inverter due to the relatively large number of switches and isolated drives required by the adopted topology. Considering that a high-quality 3 kVA inverter currently present an average price of €2100, then it is estimated that the proposed inverter can cost around 5% more. However, it is expected that cost difference can be justified by its improved characteristics.

8.2 Relevant contributions

The most relevant contributions of this work are:

- The proposed topology was implemented with modern components and experimental results showed that it can present superior performance when compared to similar high-quality inverters.
- Detailed analysis of the adopted topology is presented, giving support for future implementation and possible commercial application.
- A new method for preventing transformer-unbalancing was developed and validated.
- Software tools were developed to aid the design and simulation of high-resolution multilevel inverters.

8.3 Future work

There are several interesting topics for further research:

- The implemented controller does not take into account that the inverter output voltage can present a DC-level if the inverter feeds unsymmetrical loads, such as half-wave loads. Future implementations must include a mechanism to monitor and eliminate any possible output voltage DC-level.
- The implemented controller adjusts the output voltage amplitude by only changing the number of output levels. Future implementations might include fine adjustment of the output voltage amplitude by also altering the output voltage waveform shape.
- In this work, the correction of transformer-unbalancing was investigated only at steady-state level. Future work might study the transformer dynamics and should consider it on the controller design.
- Regarding inverter efficiency characteristic, it might be interesting to design the transformer according to a typical load profile. Also, future work should consider that no-load consumption can be even more decreased through individual optimization of auxiliary power supplies, control/measurement circuits, drivers and snubber circuits.
- Finally, it might be interesting to extend the proposed inverter operation to the connection with mini-grid systems.

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Appendix A
Table of normalized currents (N = 5)

(Estimated normalized currents at the transformer coils and output stage switches)

Output current: $I_{os} = 1.0$

Input current: I_p

Peak transformer ratio: $\Re_{pk} = 1.0$

I_n : current thought the n^{th} output stage switch.

Note that transformer secondary currents are equal to the correspondent series-switch current (odd switch).

p	I_p	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}
7	0.877	**0.806**	0.592	**0.891**	0.455	**0.972**	0.236	0.000	1.000	0.000	1.000
8	0.875	0.602	**0.798**	0.653	0.757	0.719	0.695	0.668	0.744	0.000	1.000
9	0.874	0.792	0.610	0.493	**0.870**	0.550	0.835	0.820	0.573	0.000	1.000
10	0.873	0.616	0.788	0.749	0.662	0.450	0.893	0.883	0.470	0.000	1.000
11	0.872	0.784	0.621	0.856	0.517	0.380	**0.925**	0.918	0.397	0.000	1.000
12	0.871	0.625	0.780	0.669	0.743	0.688	0.725	0.939	0.343	0.000	1.000
13	0.870	0.777	0.629	0.536	0.844	0.811	0.585	0.954	0.301	0.000	1.000
14	0.870	0.633	0.774	0.739	0.674	0.867	0.498	0.964	0.267	0.000	1.000
15	0.869	0.772	0.636	0.836	0.549	0.900	0.435	**0.971**	0.239	0.000	1.000
16	0.869	0.638	0.770	0.677	0.736	0.730	0.683	0.797	0.603	0.563	**0.826**
17	0.869	0.768	0.641	0.560	0.828	0.608	0.794	0.671	0.741	0.715	0.699
18	0.869	0.643	0.766	0.734	0.679	0.530	0.848	0.590	0.808	0.787	0.616
19	0.868	0.765	0.645	0.822	0.570	0.473	0.881	0.528	0.849	0.833	0.553
20	0.868	0.647	0.762	0.682	0.732	0.683	0.730	0.478	0.878	0.865	0.502
21	0.868	0.761	0.649	0.577	0.817	0.785	0.620	0.437	0.900	0.888	0.459
22	0.868	0.650	0.760	0.730	0.683	0.835	0.550	0.402	0.916	0.906	0.423
23	0.868	0.759	0.651	0.812	0.584	0.868	0.497	0.372	**0.928**	0.920	0.392
24	0.868	0.653	0.758	0.685	0.729	0.730	0.683	0.616	0.788	0.931	0.364
25	0.868	0.757	0.654	0.589	0.808	0.630	0.777	0.729	0.685	0.940	0.340
26	0.867	0.655	0.756	0.728	0.686	0.565	0.825	0.787	0.616	0.948	0.319
27	0.867	0.755	0.656	0.804	0.594	0.516	0.857	0.826	0.564	0.954	0.300
28	0.867	0.657	0.754	0.687	0.727	0.684	0.730	0.854	0.521	0.959	0.282
29	0.867	0.753	0.658	0.599	0.801	0.771	0.637	0.875	0.485	0.964	0.267
30	0.867	0.658	0.753	0.726	0.688	0.817	0.577	0.891	0.453	0.968	0.253
31	0.867	0.751	0.660	0.798	0.602	0.848	0.530	0.905	0.426	**0.971**	0.240

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Appendix B
Multilevel waveform design tool - user guide

1. General information

The Multilevel waveform design tool was developed in C language, using Builder 1.0 (for Windows) visual programming environment. All sources are available from the author (sdaher@secrel.com.br / daher@re.e-technik.uni-kassel.de). Main features are:

- Construction of multilevel waveforms up to 35 levels per quarter cycle, with the possibility to include user-defined hold-on-at-zero time;
- Determination of waveforms with reduced THD contents through fine adjustment of the switching angels ("improved" waveforms);
- Inclusion of configurable smoothness in waveforms with non-zero hold-on-at-zero time;
- Calculus of THD and Modulation index for all generated waveforms;
- Generation of look-up tables in C-code format for direct implementation in a microcontroller;
- Generation of waveforms text file (length: 1000 points);
- Generation of text file containing analysis data and switching angels.

2. Description of input parameters

Parameter	Description
p:	Number of levels per quarter cycle (also the number of switching angels);
INI:	First harmonic included in THD calculus;
SEL:	Last harmonic used in the calculus of the THDsel output;
X:	Last harmonic used in the calculus of the THDx output;
FREQ:	Waveform frequency;
Aref:	Defines the reference sinus (used only by the "NATURAL" command).
Tz:	Defines the user hold-on-at-zero time (in us).
Mi:	Desired value of modulation index (if equal to 0, then it is not considered).
Wmin:	minimum width of any step;
Max_Hsel:	Used by the command "MIN(X)", to define a constraint for the maximum allowed THDsel (THDsel <= Max_Hsel)
Max_Hx:	Used by the command "MIN(SEL)", to define a constraint for the maximum allowed THDx (THDx <= Max_Hx)
INT:	Defines the control interval (in us).
Step_INI:	Height of the initial step (used by the "SMOOTH" command)
Step_ADD:	Height of the additional steps (used by the "SMOOTH" command)
RAMP:	Force the commands "MIN(x)" and "MIN(sel)" to search waveforms where step widths increase gradually. RAMP is marked as default.

3. Description of commands

Parameter	Description
NATURAL	Generates a waveform based on the straightforward* method described in section 4.5.1. Used parameters: p, Mi, Aref and Tz. *In case of Mi ≠ 0, the last switching angle is adjusted to produce the specified Mi.
SMOOTH	Introduces smoothness in a waveform generated previously. Used parameters: Step_INI, Step_ADD and INT.
MIN(X)	Fine adjustment of the current waveform: search of an improved waveform with minimum value of THDx (subjected to the MAX_Hsel constraint). Used parameters: Tz, Mi, Wmin, RAMP, MAX_Hsel and INT.
MIN(SEL)	Fine adjustment of the current waveform: search of an improved waveform with minimum value of THDsel (subjected to the MAX_Hx constraint). Used parameters: Tz, Mi, Wmin, RAMP, MAX_Hx and INT.
C CODE	Generates an output text file containing the equivalent C source code for the current waveform.
MANUAL	Generates a waveform based on arbitrary values of switching angels (specified on the right side of the window: T1 - T35). Used parameter: p.
STOP	Used to stop the current search ("MIN" functions) when convergence is reached (when there is no more changes in the values of THDx or THDsel shown above the STOP button).
SAVE DATA	Save data for the current waveform.
THD WAVE	Makes the analysis of the current waveform in the screen (analysis of the graphical data points).
FILE MENU	Used to load and display waveform data in .CSV format (direct from Tektronic oscilloscope - spreadsheet format) or in .MAT format (ASCII text file, one row).

3. Example of use

Find all waveform data for p = 16, with T_z = 700us and 64 points per cycle.

- Set INT = 75 and use other parameters as defaults
- Press NATURAL
- Press MIN(X)
- Press STOP (when convergence applies)
- Press SMOOTH
- Press SAVE DATA
- Press AVRCODE
- Press SAVE DATA

Appendix C
C Source code for optimized waveforms

Hold = 700us Control interval=75.00000us
STEPS= 64 (including the first 2 steps at zero)

```
const unsigned char Shape16[]={0,0,1,2,3,3,3,4,4,4,5,5,6,6,6,7,7,7,8,8,8,9,9,9,10,10,10,10,11,11,11,12,
12,12,12,13,13,13,13,13,14,14,14,14,14,15,15,15,15,15,15,15,15,16,16,16,16,16,16,16,16,16,16,16
}; /* Tz=700.00us Int=75.00us THD50=2.80 MI=1.004*/

const unsigned char Shape17[]={0,0,1,2,3,3,4,4,4,5,5,5,6,6,7,7,7,8,8,8,9,9,9,10,10,10,11,11,11,12,12,12,
12,13,13,13,14,14,14,14,14,15,15,15,15,16,16,16,16,16,16,16,16,16,17,17,17,17,17,17,17,17,17,17
}; /* Tz=700.00us Int=75.00us THD50=2.90 MI=0.999*/

const unsigned char Shape17[]={0,0,1,2,3,3,4,4,4,5,5,5,6,6,7,7,7,8,8,8,9,9,9,10,10,10,11,11,11,12,12,12,
12,13,13,13,14,14,14,14,14,15,15,15,15,16,16,16,16,16,16,16,16,16,17,17,17,17,17,17,17,17,17,17
}; /* Tz=700.00us Int=75.00us THD50=2.90 MI=0.999*/

const unsigned char Shape19[]={0,0,1,2,3,3,4,4,5,5,6,6,7,7,7,8,8,9,9,9,10,10,11,11,11,12,12,12,13,13,13,14,
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}; /* Tz=700.00us Int=75.00us THD50=2.91 MI=1.000*/

const unsigned char Shape20[]={0,0,1,2,3,4,4,5,5,6,6,6,7,7,8,8,9,9,9,10,10,11,11,11,12,12,13,13,13,14,14,14,
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}; /* Tz=700.00us Int=75.00us THD50=2.96 MI=0.999*/

const unsigned char Shape21[]={0,0,1,2,3,4,4,5,5,6,6,7,7,8,8,9,9,9,10,10,11,11,12,12,12,13,13,14,14,14,15,15,
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}; /* Tz=700.00us Int=75.00us THD50=3.01 MI=0.996*/

const unsigned char Shape22[]={0,0,1,2,3,4,5,5,6,6,7,7,8,8,9,9,9,10,10,11,11,12,12,13,13,13,14,14,15,15,15,16,
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}; /* Tz=700.00us Int=75.00us THD50=3.04 MI=0.995*/

const unsigned char Shape23[]={0,0,1,2,3,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,14,15,15,16,16,16,
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}; /* Tz=700.00us Int=75.00us THD50=3.14 MI=0.997*/

const unsigned char Shape24[]={0,0,2,3,4,4,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,16,17,17,
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}; /* Tz=700.00us Int=75.00us THD50=2.50 MI=0.997*/

const unsigned char Shape25[]={0,0,2,3,4,5,5,6,6,7,7,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,
18,19,19,19,20,20,21,21,21,22,22,22,22,23,23,23,23,23,24,24,24,24,24,25,25,25,25,25,25,25,25,25
}; /* Tz=700.00us Int=75.00us THD50=2.58 MI=0.998*/

const unsigned char Shape26[]={0,0,2,3,4,5,5,6,7,7,8,8,9,9,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,
19,19,20,20,21,21,21,22,22,22,23,23,23,24,24,24,24,24,25,25,25,25,25,26,26,26,26,26,26,26,26,26
}; /* Tz=700.00us Int=75.00us THD50=2.63 MI=0.997*/

const unsigned char Shape27[]={0,0,2,3,4,5,6,6,7,7,8,9,9,10,10,11,12,12,13,13,14,14,15,15,16,17,17,17,18,18,19,19,
20,20,21,21,21,22,22,23,23,23,24,24,24,24,25,25,25,25,26,26,26,26,26,26,27,27,27,27,27,
27,27,27}; /* Tz=700.00us Int=75.00us THD50=2.68 MI=0.996*/
const unsigned char Shape28[]={0,0,2,3,4,5,6,6,7,8,8,9,10,10,11,11,12,13,13,14,14,15,15,16,17,17,18,18,19,19,
20,20,21,21,21,22,22,23,23,23,24,24,24,25,25,25,26,26,26,26,27,27,27,27,27,27,28,28,
28,28,28,28,28,28}; /* Tz=700.00us Int=75.00us THD50=2.71 MI=0.997*/

const unsigned char Shape29[]={0,0,2,3,4,5,6,7,7,8,9,9,10,11,11,12,12,13,14,14,15,15,16,17,17,18,18,19,19,
20,20,21,21,22,22,23,23,23,24,24,25,25,25,26,26,26,27,27,27,27,28,28,28,28,28,28,29,29,29,29,29,29,
29,29}; /* Tz=700.00us Int=75.00us THD50=2.75 MI=0.998*/

const unsigned char Shape30[]={0,0,2,3,4,5,6,7,8,8,9,10,10,11,12,12,13,14,14,15,15,16,17,17,18,18,19,19,
20,21,21,22,22,22,23,23,24,24,25,25,26,26,26,27,27,27,28,28,28,28,29,29,29,29,29,29,30,30,30,30,30,30,
30,30}; /* Tz=700.00us Int=75.00us THD50=2.82 MI=0.999*/

const unsigned char Shape31[]={0,0,2,3,4,5,6,7,8,9,9,10,11,11,12,13,13,14,15,15,16,17,17,18,18,19,
20,20,21,21,22,22,23,23,24,24,25,25,26,26,26,27,27,27,28,28,28,29,29,29,29,30,30,30,30,30,31,31,
31,31,31,31,31,31}; /* Tz=700.00us Int=75.00us THD50=2.85 MI=0.998*/
```

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Appendix D
Microcontroller firmware

```
//=============================================================
// PA0: Ib            PB0: LCD RS       PC0: S1          PD0: UART RX
// PA1: Vb            PB1: LCD EN       PC1: S2          PD1: UART TX
// PA2: Vo            PB2: LCD D4/TEC   PC2: S3          PD2: Short-Det.
// PA3: NC            PB3: LCD D5/TEC   PC3: S4          PD3: Hab.Drives
// PA4: Temp          PB4: LCD D6/TEC   PC4: S5          PD4: Sa
// PA5: Ip            PB5: LCD D7       PC5: S6          PD5: Sb
// PA6: ucaux(out)    PB6: S9           PC6: S7          PD6: Sc
// PA7: ucaux(in)     PB7: S10          PC7: S8          PD7: Sd
//=============================================================
//=============================================================
// Controls:
// MODE:  (Output voltage control flag. Used also for proposital disbalancement)
//              0 = MANUAL;
//       x = AUTOMATIC;
//
// FBAL:  (Mode of banlancement. See also IBAL.)
//              0 = MANUAL;
//       1 = AUTOMATIC;
//       3 = PROPOSITAL DISBALANCEMENT (DECREASES POSITIVE SEMI-CYCLE)
//       4 = PROPOSITAL DISBALANCEMENT (DECREASES NEGATIVE SEMI-CYCLE)
//
// IBAL:  (Only valid if FBAL=0. For others values, FBAL is fixed to 0 or is automatic)
//              0 = NO BANCEMENT
//       1 = BALANCEMENT IN POSITIVE SEMI-CYCLE ONLY
//       2 = BALANCEMENT IN POSITIVE SEMI-CYCLE ONLY
//       3 = BALANCEMENT IN BOTH SEMI-CYCLES
//       7 = All full bridge switches are oppened during all dead times.
//
// CMUX:  (Output stage control flag.)
//              0: All output swicthes are always openned.
//              1: Output is always short-circuited.
//              2: Normal operation.
//
// Pdelay: Controls "zero time" of the full bridge.
//
// Shape:  Controls number of levels of the output voltage. Also controls
//       output voltage value.
//       0 ==> 16 levels;    15 ==> 31 levels.
//
//
//=============================================================
// ERROR MAP
//=============================================================
// ERROR:  0x01 = Auxiliar Microcontroller ERROR
//       0x02 = Overcurrent (Hardware)
//       0x04 = I16 (1.2ms) Overcurrent
//       0x08 =
//       0x10 =
//       0x20 =
//       0x40 =
//       0x80 =
//
// ERRORM: 0x01 = RESET
//       0x02 = BAT LOW
//       0x04 = Undervoltage  (Output)
//       0x08 = Overvoltage   (Output)
//       0x10 = Over current  (one cycle)
//       0x20 =
//       0x40 =
//=============================================================
// EEPROM MAP
//=============================================================
// 0 = Voltage Setpoint
// 2 = Grid (1 or 0)
// 3 = EMASK
// 4 = MODE (Manual/Auto)
//
// 10 = Voltage Gain   (Calibration)
// 12 = Current Gain   (Calibration)
// 14 = Current Offset (Calibration)
//
```

```
// 40 = Voltage Limiting (Protection)
// 42 = Current Limitation 1.2ms (Protection)
// 44 = Current Limitation 1 sec (Protection)
//=============================================================
#define OFFIbatINI   256
#define GAIN_IBAT_INI   99
#define GAIN_VOLT_INI   93

#define DEFAULT_MODE    1

#define Tdead                   1

#define VBATMIN                 360
#define VBATMAX                 620
#define VOUT_MIN        150
#define VOUT_RATED                      230
#define VOUT_MAX        253
#define LIMIT_I16_INI   3500
#define LIMIT_I16_MAX   5000
#define LIMIT_IMED_INI          1400
#define LIMIT_IMED_MAX      2500

#define FB_DELAY                0

#define MUX_INI         2
#define MUX_DEFAULT                     0

#define Kp_INI                  4
#define Ki_INI                  7
#define PI_MIN                          1
#define MAX_CORRECTION  233
#define LIMINST         30
#define CORINST         MAX_CORRECTION - 3
#define FACTOR_SI       4
#define MAX_SI          FACTOR_SI*MAX_CORRECTION

#define START_SPEED                                     7
#define Instant_MUXON                           1025
#define Instant_CONTROL_ON                              Instant_MUXON + 2
#define MAX_START_COUNT                                 1200

#include <io8535.h>
#include <macros.h>
#define setbit(ADDRESS,BIT) (ADDRESS |= (1<<BIT))
#define clearbit(ADDRESS,BIT) (ADDRESS &= ~(1<<BIT))
#define checkbit(ADDRESS,BIT) (ADDRESS & (1<<BIT))
//=============================================================
// Tabel
//=============================================================
const unsigned char Shape15[]={ 2,4,5,6,6,7,8,8,9,10,10,11,12,12,13,14,
14,15,15,16,17,17,18,18,19,20,20,21,21,22,22,23,
23,24,24,25,25,25,26,26,27,27,27,28,28,28,28,29,
29,29,29,30,30,30,30,30,31,31,31,31,31,31,31,31
};

const unsigned char Shape14[]={ 2,4,5,5,6,7,7,8,9,9,10,11,11,12,13,13,
14,14,15,16,16,17,17,18,18,19,19,20,20,21,21,22,
22,23,23,24,24,25,25,25,26,26,26,27,27,27,28,28,
28,28,29,29,29,29,29,29,30,30,30,30,30,30,30,30
};

const unsigned char Shape13[]={ 2,4,5,5,6,6,7,8,8,9,10,10,11,12,12,13,
13,14,14,15,16,16,17,17,18,18,19,19,20,20,21,21,
22,22,23,23,23,24,24,24,25,25,25,26,26,26,27,27,
27,27,28,28,28,28,28,28,29,29,29,29,29,29,29,29
};

const unsigned char Shape12[]={ 2,4,4,5,6,6,7,7,8,9,9,10,11,11,12,12,
13,13,14,15,15,16,16,17,17,18,18,19,19,20,20,20,
21,21,22,22,23,23,23,24,24,24,25,25,25,25,26,26,
26,26,27,27,27,27,27,27,28,28,28,28,28,28,28,28
};

const unsigned char Shape11[]={ 2,4,4,5,5,6,7,7,8,8,9,10,10,11,11,12,
12,13,13,14,15,15,16,16,17,17,18,18,18,19,19,20,
20,21,21,21,22,22,22,23,23,23,24,24,24,25,25,25,
25,25,26,26,26,26,26,26,27,27,27,27,27,27,27,27
```

```
};

const unsigned char Shape10[]={ 2,3,4,5,5,6,6,7,8,8,9,9,10,10,11,11,
12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,19,
19,20,20,21,21,21,22,22,22,23,23,23,23,24,24,24,
24,25,25,25,25,25,25,25,26,26,26,26,26,26,26,26
};

const unsigned char Shape09[]={ 2,3,4,4,5,6,6,7,7,8,8,9,9,10,10,11,
11,12,12,13,13,14,14,15,15,16,16,17,17,17,18,18,
19,19,19,20,20,20,21,21,21,22,22,22,22,23,23,23,
23,24,24,24,24,24,24,24,25,25,25,25,25,25,25,25
};

const unsigned char Shape08[]={ 2,3,4,4,5,5,6,6,7,7,8,9,9,10,10,11,
11,12,12,12,13,13,14,14,15,15,16,16,16,17,17,18,
18,18,19,19,19,20,20,20,21,21,21,21,22,22,22,22,
22,23,23,23,23,23,23,23,24,24,24,24,24,24,24,24
};

const unsigned char Shape07[]={ 2,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,
11,11,11,12,12,13,13,14,14,15,15,15,16,16,16,17,
17,18,18,18,19,19,19,19,20,20,20,20,21,21,21,21,
22,22,22,22,22,22,22,23,23,23,23,23,23,23,23,23
};

const unsigned char Shape06[]={ 2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,
10,11,11,11,12,12,13,13,13,14,14,15,15,15,16,16,
16,17,17,17,18,18,18,19,19,19,19,20,20,20,20,20,
21,21,21,21,21,21,21,22,22,22,22,22,22,22,22,22
};

const unsigned char Shape05[]={ 2,3,3,4,4,5,5,6,6,7,7,7,8,8,9,9,
10,10,10,11,11,12,12,12,13,13,14,14,14,15,15,15,
16,16,16,17,17,17,17,18,18,18,18,19,19,19,19,19,
20,20,20,20,20,20,20,21,21,21,21,21,21,21,21,21
};

const unsigned char Shape04[]={ 2,3,3,4,4,4,5,5,6,6,7,7,8,8,8,9,
9,10,10,10,11,11,12,12,12,13,13,13,14,14,14,15,
15,15,16,16,16,16,17,17,17,17,18,18,18,18,18,19,
19,19,19,19,19,19,20,20,20,20,20,20,20,20,20,20
};

const unsigned char Shape03[]={ 2,3,3,3,4,4,5,5,6,6,6,7,7,8,8,8,
9,9,9,10,10,11,11,11,12,12,12,13,13,13,14,14,
14,14,15,15,15,16,16,16,16,16,17,17,17,17,17,18,
18,18,18,18,18,18,19,19,19,19,19,19,19,19,19,19
};

const unsigned char Shape02[]={ 2,2,3,3,4,4,4,5,5,6,6,6,7,7,8,8,
8,9,9,9,10,10,10,11,11,11,12,12,12,13,13,13,
13,14,14,14,14,15,15,15,15,16,16,16,16,16,16,17,
17,17,17,17,17,17,18,18,18,18,18,18,18,18,18,18
};

const unsigned char Shape01[]={ 2,2,3,3,3,4,4,5,5,5,6,6,6,7,7,7,
8,8,8,9,9,9,10,10,10,11,11,11,12,12,12,12,
13,13,13,13,14,14,14,14,15,15,15,15,15,15,16,16,
16,16,16,16,16,17,17,17,17,17,17,17,17,17,17,17
};

const unsigned char Shape00[]={ 2,2,3,3,3,4,4,4,5,5,5,6,6,6,7,7,
7,8,8,8,9,9,9,10,10,10,10,11,11,11,11,12,
12,12,12,13,13,13,13,13,14,14,14,14,14,15,15,15,
15,15,15,15,15,16,16,16,16,16,16,16,16,16,16,16
};

//=============================================================
// Constants
//=============================================================
// Global Variables
//=============================================================
  int i,j;                                                    // General Purpose Integers (main)


  unsigned char c,d,dado;                                     //
```

```
  unsigned char Pdelay=FB_DELAY;          // Delay - Bridge
  unsigned char Shape=0;                                  // Waveform Selection (0 to 15)
  unsigned char ONOFF=0;                                                  // ON/OFF flag: 0=OFF
  unsigned int  Cstart=MAX_START_COUNT;          // Start-up counter
  unsigned char Cpdown=0;                                                 // Power down counter
  unsigned char CMUX=MUX_DEFAULT;                                         // MUX Control
  unsigned char MODE=DEFAULT_MODE;                              // Control Mode (Auto=1 or Manual=0)
  unsigned char ERROR=0;                  // System Status (Errors)
  unsigned char ERRORM=1;                 // System Status (Errors in Main)
                                                                          // 1=RESET 2=BATLOW 4= 8=
                                                                          // 10= 20= 40= 80=
  unsigned char Menu=1;        // Save last Menu
  unsigned char Tctr=0;        // Time flag - Control Program

  unsigned int Ad_Ibat,Ad_Vbat; // AD Conversion Results
  unsigned int Ad_Vout;                   // AD Conversion Results : Output voltage
  unsigned int Vmed=0,Imed=0,Vbat;  // Average values (module everage)
  unsigned int Vout=0;                                    // Real value of output voltage
  unsigned int Iin=0;                     // Real value of input current
  unsigned int IW=0;                      // Average Active Current

  unsigned int  Vset=VOUT_RATED;                   //CFG: Voltage Setpoint

  unsigned int  LI16=LIMIT_I16_INI;  //CFG: Current Limitation (instantaneos)
  unsigned int  LIin=LIMIT_IMED_INI;  //CFG: Current Limitation (Mean one Cycle)
  unsigned int  LVout=VOUT_MAX;  //CFG: Volt. Lim.(safety) (steady state)

  unsigned int  Ioffset=OFFIbatINI;          //CFG: Calibration Parameter
  unsigned int  Vgain=GAIN_VOLT_INI;                //CFG: Calibration Parameter
  unsigned char cBatBad=0;                // Counter to select number of out of range Bat. Volt.

  unsigned char IBal=0;                   // Indicates Direction of Balance Correction
  unsigned char FBal=1;                   // Mode of Balance Manegement

  int Verro;                                                      // Used by Control Algorithm (Voltage Control)
  int PIerro;                                                     // Disbalancement error
  int SI=0;                                               // Integral Part of the controller
  int Ki=Ki_INI;                                          // Integral Gain
  int Kp=Kp_INI;                                          // Integral Gain
  unsigned char PI1=PI_MIN,PI2=PI_MIN; // Balancing Values (balance controller outputs)
  unsigned char PI1a,PI2a;
  int MAX_COR=MAX_CORRECTION;   // Mac possible value for PI
//=============================================================
// Variables for Interrupt Routine (TIMER2)
//=============================================================
  unsigned char INT_MODOMUX=MUX_DEFAULT;                  // MUX Control (Interrupt)
  unsigned char Ic256=0;                                  // Counter 0 to 255
  unsigned char Ic64=0;                                   // Counter  0  to 63 (64 steps)
  unsigned char Ic64x=0;                                  // Counter (0 to 63) or (63 to 0)
  unsigned char Ic3=0;             // Counter  0  to 3 (4 steps)
  unsigned char Mux1=0,Mux2=0;             // Current MUX states
  unsigned char Mux1a=0,Mux2a=0;           // Last MUX states
  unsigned char Iaux;                                     // Auxiliar for Interrupt
  unsigned char IShape=0;          // Waveform Selection (0 to 15)(Interrupt use)
  unsigned char IPdelay=63;        // Delay - Bridge (Interrupt use)
  unsigned char Level=0;           // Current Output Level
  unsigned char STOPC=100;                                // Startup Counter  (INT)
  unsigned char Iucaux=0;          // Last ucaux State
  unsigned char IFaux=0;           // uaux Falt Detector

  unsigned int  II=0;                                     // Instantaneos Current (Module)
  unsigned int  IVmed=0,IImed=0;           // Average values
  unsigned int  II16=0;                                   // Instantaneos Current
  unsigned char Ic16=0;            // Counter 0 to 16
  unsigned char Is1=0;                                            // To Detect unbalancing
  unsigned char Is2=0;                                            // To Detect unbalancing

  unsigned char cpuv;                                     // Used by undervoltage protection
  unsigned char CMUXINI=MUX_INI;
  unsigned char TMR2tmp;
  unsigned char Flag_Msat=1;
//-----------------------------------------------------------------------
// Calculate Initial Shape based on Battery voltage and output voltage
//-----------------------------------------------------------------------
//unsigned char Calc_Shape_Ini()
//{
```

```
//              unsigned char sh;
//              unsigned char dif;
//
//   if(Vbat<=410)sh=15;
//   else sh = 15 - (((Vbat/10)-41)*7)/11;
//   if(sh>15)sh=15;                                          // Overflow em Shape
//   return(sh);
//}


//=============================================================
// Delay Function (with Priority tasks inside)
//=============================================================
void delay(unsigned int at)
{


 while(at--){
  if(Tctr){
      Tctr=0; // Clear time flag (will be set by interrupt)
 //-------------------------------------------------------------
 // Balance Controller
      if(FBal==1){                                              // Automatic Balancement Control
              PIerro = Is1 - Is2;                       // Disbalancement error (controller input)
          SI = SI + PIerro*Ki;
              if(SI>MAX_SI)SI=MAX_SI;
              if(SI<-MAX_SI)SI=-MAX_SI;
              PIerro = PIerro*Kp + SI/FACTOR_SI;
              if(PIerro>=(MAX_COR-3)) PIerro = MAX_COR-3;
          if(PIerro<=-(MAX_COR-3))PIerro = -(MAX_COR-3);
              if(PIerro<0){
                  PIerro=-PIerro;
                  if(PIerro<PI_MIN)PIerro=PI_MIN;      // Minimum allowed correction
                          PI1 = PI_MIN;
                          PI2 = PIerro;
          }
              else{
                  if(PIerro<PI_MIN)PIerro=PI_MIN;              // Minimum allowed correction
                          PI2 = PI_MIN;
                          PI1 = PIerro;
              }
              IBal = 1;
    }
      else if(FBal)IBal = 0;                                    // Mode 0: Manual Mode
 //-------------------------------------------------------------
 // Power Down Handling
    if(Cpdown<250)Cpdown++;
      if(Cpdown>50){
     PORTD&=0x0F;     // Turn off all Full-Bridge MOS
     PORTC=0x00;      // Turn off MUX SWs 1 - 18
     PORTB&=0x3F;     // Turn off MUX SWs 19 and 20
    }
 //-------------------------------------------------------------
 // Real values calculus
    Vout =  ((Vmed>>7)*Vgain)/100;
    Iin  =     ((Imed>>4)*5)/4;                       // Imed = 125 measurements (2^7)
    Vbat =  (Ad_Vbat*50)/(76);         //  10.0V = 149
 //-------------------------------------------------------------
 // Batterie Voltage Handling
      if((Vbat<VBATMIN)||(Vbat>VBATMAX)){
        cBatBad++;
        if(cBatBad>1)ERRORM|=0x02;
    }
      else  cBatBad=0;

 //-------------------------------------------------------------
 // Overvoltage error handling
   if(Vout>270)ERRORM|=0x08;       // Overvoltage error
 //-------------------------------------------------------------
 // Overcurrent error handling
      if(Iin > LIin)ERRORM|=0x10;
 //-------------------------------------------------------------
 // Startup Handling and Error Handling(Stand-Alone Mode)
      if(STOPC<3){
        if(Cstart<MAX_START_COUNT){
          Cstart+=START_SPEED;
          if(Cstart>=Instant_MUXON){ // turn on output
```

```
                CMUX=CMUXINI;         // 0=OFF 1=short 2=normal
              }
          Pdelay = 64 - (Cstart>>4);                                          // increases duty gradually
              if(Pdelay<FB_DELAY)Pdelay=FB_DELAY;
              if(Pdelay>64)Pdelay=FB_DELAY;
              cpuv=1;
        }
        else{
      // Undervoltage error handling
          if((Vout<VOUT_MIN)&&(CMUX==2)&&(MODE)&&(cpuv))ERRORM|=0x04;
        }
      }
 //---------------------------------------------------------------
 // Controller (Stand-Alone Mode)
      if(MODE){
      if(Cstart<Instant_CONTROL_ON){     // if it is starting, see only battery
//                Shape = Calc_Shape_Ini();
                  Shape = 0;
        }
        else{                                 // After Startup - Feedback Control
          Verro = (int)Vout - (int)Vset;
              if(Verro<=-6)if(Shape<15)Shape++; // Torelance of 7V
              if(Verro>=6)if(Shape)Shape--;  // Torelance of 7V
              if(CMUX<2)Shape = 0;                          // Output is forced to float or is short-circ.
        }
      }
 //---------------------------------------------------------------



 //---------------------------------------------------------------
 // Error Handling
      if(ERRORM)if(STOPC<3)ONOFF=0;
 //---------------------------------------------------------------
  }// Closes if(Tctr)
 } // Closes while(at--);
// if(checkbit(USR,RXC))trata_serial();
}
//=================================================================
//=================================================================
// Libraries
//=================================================================
#include "lcd.bli"
#include "keyboard.bli"
#include "eeprom.bli"
//=================================================================



//---------------------------------------------------------------
// MAIN
//---------------------------------------------------------------
void main(void)
{
 CLI(); //disable all interrupts
//-------------------------------- Configuracoes das Portas
 PORTA = 0x00;       // PORTA A:
 DDRA  = 0x40;  // A/D e Uaux

 PORTB = 0x3F;  // PORTA B:
 DDRB  = 0xFF;  // LCD, Teclado e 2 MOS

 PORTC = 0x00;       // PORTA C: MOS
 DDRC  = 0xFF;  //

 PORTD = 0x0F;  // PORTA D:
 DDRD  = 0xFA;  // Serial, Short Det., Hab. and FB SWs
//-------------------------------- Configuracao do Timer 2
 TCCR2 = 0x00; // stop
 ASSR =  0x00; // set async mode
 TCNT2 = 0xBB; // setup
 OCR2  = 104;  // 0x45 = 50us  0x8A = 100us  92 = 66.55us 108=78.125us
 TCCR2 = 0x0A; // start (prescaler=8)
//-------------------------------- Configuracao da Serial
```

```
 UCR  = 0x00; //disable while setting baud rate
 UBRR = 5;    //set baud rate 11.0592  143=4800 5=115200
 UCR  = 0x18; //enable
//------------------------------- Configuracao do AD
 ADCSR = 0xC3;  // CFG AD: Prescaler = 0x03
//------------------------------- Configuracao das Interrupcoes
 MCUCR = 0x02;  // INT0 triggers on falling edge
 GIMSK = 0x40;  // Enable external interrupt 0
 TIMSK = 0x80;  // Habilita interrupcao do Timer 2
 SEI();                     // re-enable interrupts

//=============================================================
// LOAD USER CONFIGURATION (FROM EEPROM MEMORY)
//=============================================================
//  Vset  = EErdInt(0);
//  if(Vset>300)Vset=230;    // Voltage Setpoint

//  MODE  = EErdByte(4);
//  if(MODE>250)MODE=1;                        // Control MODE (1=AUTO 0=MANUAL)

//  Vgain = EErdInt(10);
//  if(Vgain>100)Vgain=93;            //

//  Igain = EErdInt(12);
//  if(Igain>100)Igain=82;            //

//  Ioffset=EErdInt(14);
//  if(Ioffset>500)Ioffset=OFFIbatINI; //

//  LVout = EErdInt(40);
//  if(LVout>270)LVout=270;

//  LI16  = EErdInt(42);
//  if(LI16>LIMIT_I16)LI16=LIMIT_I16;

  //LI1s  = EErdInt(44);if(LI1s>100)LI1s=1400;

//=============================================================
// MAIN LOOP: HUMAN-MACHINE INTERFACE
//=============================================================
 while(1){
//------------ Main Screen (STATUS) -----------------------------
mainscreen:
   configura_lcd();
   while(1){
    linha1();
       if(ONOFF==1)epal_lcd("ON ");else epal_lcd("-- ");
       mostra_hexabyte(ERROR);ed_lcd(' ');
    mostra_hexabyte(ERRORM);

    linha2();
    enum_lcd(Vbat,3,0,1);ed_lcd(' ');
       enum_lcd(Iin,4,0,1);ed_lcd(' ');
       enum_lcd(Vout,3,0,0);
       i = le_teclado(0);
       if(i==3){apaga_lcd();goto menuscreen;}
       if(i==2){
          if(ONOFF)ONOFF=0;
          else{
                Pdelay=63;
                Shape=0;
            ONOFF=1;
          }
          delay(3000);
       }
   }
//------------ Menu Screen (Selection) ---------------------------
menuscreen:
   linha1();        // ________________ // 16 Characters
   if(Menu==0)epal_lcd("MAIN");else
   if(Menu==1)epal_lcd("TEST");else
   if(Menu==2)epal_lcd("DEBG");else
//    if(Menu==3)epal_lcd("CFG CALIBRATION");else
   if(Menu==3)epal_lcd("OPTI");
   else
                              epal_lcd("PTEC");
   linha2();
```

```
  if(entra_byte_live(&Menu,2,0,4,1)==0)goto menuscreen;
  apaga_lcd();
  if(Menu==0)goto mainscreen;
  if(Menu==1)goto testscreen;
  if(Menu==2)goto debugscreen;
  if(Menu==3)goto cfgOptions;
//  if(Menu==3)goto cfgProtections;
//  else      goto cfgCal;
goto menuscreen;   // still in loop until ENTER is pressed
//------------ Debug Screen --------------------------------------------
debugscreen:
  delay(10000);
debug1:
  linha1();
  mostra_hexabyte(Is1);ed_lcd('/');  // Peak mag. current (POSITIVE semi-cycle)
  mostra_hexabyte(Is2);ed_lcd(' ');  // Peak. mag. current (NEGATIVE semi-cycle)
  mostra_hexabyte(PI1); ed_lcd('/'); // Controller Variable
  mostra_hexabyte(PI2);                                    // Controller Variable
//  linha2();
//  enum_lcd(Iin,4,0,1);ed_lcd(' ');   // Input Current
//  enum_lcd(debug,4,0,0);ed_lcd(' ');  debug = 0; // I16 max.
//  enum_lcd(Vbat,3,0,1);                          // Battery Voltage


  i = le_teclado(0);
  if(i==3)goto mainscreen;
goto debug1;


//------------ Advanced Test Screen ---------------------------------------
testscreen:
  apaga_lcd();
  epal_lcd("D:");        entra_byte_live(&Pdelay,2,0,63,0);    // Fixed Delay
  epal_lcd("S:");        entra_byte_live(&Shape,2,0,15,0);          // Shape (only manual)
  epal_lcd("B:");        entra_byte_live(&FBal,1,0,5,0);            // Type of Balancement
                                                          entra_byte_live(&Flag_Msat,1,0,1,0);       // Unbancing Meas. Selection
  cpuv=0;                                                          // disable under-voltage error
  epal_lcd("M:");entra_byte_live(&CMUX,1,0,2,0);
  CMUXINI=CMUX;
  cpuv=1;                                                          // enable under-voltage error

  linha2();
  epal_lcd("B:");       entra_byte_live(&IBal,1,0,7,0);
  epal_lcd("P1:");      entra_byte_live(&PI1,3,1,250,0);
  epal_lcd("P2:");      entra_byte_live(&PI2,3,1,250,0);

goto mainscreen;
//------------ Config Screen (OPTIONS) --------------------------
cfgOptions:
  apaga_lcd();
//  epal_lcd("M:");
  entra_byte_live(&MODE,2,0,200,0);
//  epal_lcd("Ki:");
  read_int(&Ki,3,1,100,0,1);
  read_int(&Kp,3,1,100,0,1);

//  epal_lcd("MC:");read_int((int*)&MAX_COR,3,30,250,0,1);
//  apaga_lcd(); epal_lcd("S:"); read_int((int*)&Vset,3,195,265,0,1);
//  EEwrInt(0,Vset);
//  EEwrByte(4,MODE);
goto mainscreen;

//------------ Config Screen (Calibration) ------------------------
//cfgCal:
  // linha1(); epal_lcd("Vgain:");read_int((int*)&Vgain,3,1,100,0,1);
  // linha1(); epal_lcd("Igain:");read_int((int*)&Igain,3,1,120,0,1);
  // linha1(); epal_lcd("Ioffset:");read_int((int*)&Ioffset,3,200,300,0,1);
  // EEwrInt(10,Vgain);
  // EEwrInt(12,Igain);
  // EEwrInt(14,Ioffset);
//goto mainscreen;

//------------ Config Screen (Protections) ------------------------
cfgProtections:
/*  apaga_lcd();
  epal_lcd("I16:");
  read_int((int*)&LI16,4,10,LIMIT_I16_MAX,0,25);
```

```
  linha2();
  epal_lcd("Iin:");
  read_int((int*)&LIin,4,5,LIMIT_IMED_MAX,1,10);
  */
  //apaga_lcd(); epal_lcd("LI1s:");  read_int((int*)&LI1s,4,5,1500,1);
  //apaga_lcd(); epal_lcd("LVout:"); read_int((int*)&LVout,3,5,1500,0,3);

  //EEwrInt(40,LVout);
  //EEwrInt(42,LI16);
  //EEwrInt(44,LI1s);

goto mainscreen;

//=================================================================
// END MAIN LOOP: HUMAN-MACHINE INTERFACE
//=================================================================
 } // Closes while(1)
}  // Closes main


//-----------------------------------------------------------------
// INTERRUPT: INT0 (external - falling edge)
//-----------------------------------------------------------------
#pragma interrupt_handler int0_isr:2
void int0_isr(void)
{
 setbit(PORTD,3);      // Turn Drives OFF

 PORTD&=0x0F;                    // Turn off all Full-Bridge MOS

 ONOFF=0;                                          // Turn off Control
 ERROR|=0x02;                                 // Report error

 setbit(GIFR,INTF0);    // clear interrupt flag
}


//-----------------------------------------------------------------
// INTERRUPCAO: TIMER2
//-----------------------------------------------------------------
#pragma interrupt_handler timer2_comp_isr:4
void timer2_comp_isr(void)
{
      static int tempo=0;
//---------------------------------------------------------------------
//  FB Switching
if(STOPC==0){
   if(Ic64x==IPdelay){
      if(Flag_Msat) ADMUX = 0x05;  // Select channel: Trafo Current
      else          ADMUX = 0x00;  // Select channel: Input Current
      Ad_Ibat=3;while(Ad_Ibat--);  // Sample Time
      ADCSR |= 0x40;              //Start conversion
      while(!(ADCSR & BIT(ADIF))); //Check if convertion is ready
    Ad_Ibat=(ADCL>>1);          //Read 8 low bits first (important)
    Ad_Ibat|=(int)ADCH << 7;     //Read 2 high bits and shift into top byte
    if(Ad_Ibat>=Ioffset)II=Ad_Ibat-Ioffset;
    else                                        II=Ioffset-Ad_Ibat;

      if(Ic3==0){ // Begining of Positiv cycle
            if(FBal==3){Iaux=MODE;while(Iaux--);}                  // (3 ==> 5 us) Proposital Disbalancement (debug)
            clearbit(PORTD,5); Iaux=Tdead;while(Iaux--);  // Sw2=OFF
            setbit(PORTD,4);                                                                  // Sw1=ON
      clearbit(PORTD,6); Iaux=Tdead;while(Iaux--);  // Sw3=OFF
            setbit(PORTD,7);                                                                 // Sw4=ON
    }
    if(Ic3==2){ // Begining of Negativ cycle
            asm("nop");asm("nop");                                                                        //          Fine          balancement
(compensates software assymetry)
         if(FBal==4){Iaux=MODE;while(Iaux--);}                     // (3 ==> 5 us) Proposital Disbalancement (debug)
            clearbit(PORTD,7); Iaux=Tdead;while(Iaux--); // Sw4=OFF
            setbit(PORTD,6);                                                                 // Sw3=ON
         clearbit(PORTD,4); Iaux=Tdead;while(Iaux--); // Sw1=OFF
            setbit(PORTD,5);                                                                 // Sw2=ON
    }
    if(Ic3==1){ // End of Positiv cycle
      if(IBal){
          TMR2tmp=TCNT2;
```

```
      if(II>LIMINST){PI1a=CORINST;  PI2a=PI_MIN; }
            else{        PI1a=PI1;     PI2a=PI2;}
            Iaux=PI2a;                                                          // Balancing time
            while(Iaux--){
               asm("nop");asm("nop");asm("nop");              // Increase balancing time
               asm("nop");asm("nop");asm("nop");              // Increase balancing time
            }
            clearbit(PORTD,4);                                                  // Sw1=OFF
            clearbit(PORTD,7);                                                  // Sw4=OFF
            if(IBal==7)goto allbal;
            Iaux=PI1a;                                                          // Balancing time
            while(Iaux--){
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
         setbit(PORTD,5);                                                       // Sw2=ON
            setbit(PORTD,7);                                                    // Sw4=ON
         Iaux=(MAX_COR - PI1a - PI2a);                  // To make total time fixed
            while(Iaux--){
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
       TCNT2=TMR2tmp;
      }
      else{
         TMR2tmp=TCNT2;
         clearbit(PORTD,4); Iaux=Tdead;while(Iaux--); // Sw1=OFF
            setbit(PORTD,5);                                    // Sw2=ON
            Iaux=MAX_COR;                                                       // Balancing time
            while(Iaux--){
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
               asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
       TCNT2=TMR2tmp;
      }
      Is1=II;
    }
    if(Ic3==3){ // End of Negativ cycle
      if(IBal){
            TMR2tmp=TCNT2;
            if(II>LIMINST){PI2a=CORINST;  PI1a=PI_MIN;}
            else{        PI1a=PI1;     PI2a=PI2;}
            Iaux=PI1a;                                                          // Balancing time
            while(Iaux--){
              asm("nop");asm("nop");asm("nop");              // Increase balancing time
              asm("nop");asm("nop");asm("nop");              // Increase balancing time
            }
         clearbit(PORTD,6);                                                     // Sw3=OFF
                  clearbit(PORTD,5);                                            // Sw2=OFF
            if(IBal==7)goto allbal;
            Iaux=PI2a;                                                                  //
Balancing time
            while(Iaux--){
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
         setbit(PORTD,5);                                                       // Sw2=ON
            setbit(PORTD,7);                                                    // Sw4=ON
            Iaux=(MAX_COR - PI2a - PI1a);                                       // To make total time fixed
            while(Iaux--){
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
         TCNT2=TMR2tmp;
      }
      else{
            TMR2tmp=TCNT2;
         clearbit(PORTD,6); Iaux=Tdead;while(Iaux--);  // Sw3=OFF
            setbit(PORTD,7);                                    // Sw4=ON
            Iaux=MAX_COR;                                 // Balancing time
            while(Iaux--){
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
              asm("nop");asm("nop");asm("nop");                 // Increase balancing time
            }
         TCNT2=TMR2tmp;
      }
      Is2=II;
```

```
    }
     } // closes if(Ic64x...
}   // closes if(STOPC==0)
allbal:
//---------------------------------------------------------------------
// Ucaux Protocol
 setbit(PORTA,6);                                                    // Output Pulse to uaux

 Iaux=PINA&0x80;
 if(Iaux==Iucaux)IFaux++;
 else                                IFaux=0;
 Iucaux=Iaux;
 if(IFaux>2)ERROR|=0x01;
//---------------------------------------------------------------------
// Error Processing
 if(STOPC==25){       // RESET (0,5 sec. before start)
        ERROR=0;
        ERRORM=0;
        Cstart=0;
        CMUX=MUX_DEFAULT;         // MUX DEFAULT STATE
        Mux1a=0;
        Mux2a=0;
 }
 if(STOPC<3)if(ERROR)ONOFF=0;   // Stop System
 if(STOPC==1){
   clearbit(PORTD,3);  // Turn Drives ON
   SI = 0;                          // Inialize controller integral
     Is1 = 0;                              // Inialize measurement
     Is2 = 0;                              // Inialize measurement
 }
 if(ONOFF==0){                                                       // If system is OFF
    STOPC=200;                  // Start-up Time = 4 seconds
    setbit(PORTD,3);          // Turn Drives OFF
    PORTD&=0x0F;                                        // Turn off all Full-Bridge MOS
 }
 else{
       Cpdown=0;
 }
//---------------------------------------------------------------------
// INT.TIMER2: WaveShape Selection (table look up - SAA)
    if(IShape&0x08)
     if(IShape&0x04)
      if(IShape&0x02)
       if(IShape&0x01)Level=Shape15[Ic64x];
         else         Level=Shape14[Ic64x];
        else
       if(IShape&0x01)Level=Shape13[Ic64x];
         else         Level=Shape12[Ic64x];
     else
        if(IShape&0x02)
       if(IShape&0x01)Level=Shape11[Ic64x];
         else         Level=Shape10[Ic64x];
        else
       if(IShape&0x01)Level=Shape09[Ic64x];
         else         Level=Shape08[Ic64x];
     else
     if(IShape&0x04)
      if(IShape&0x02)
       if(IShape&0x01)Level=Shape07[Ic64x];
         else         Level=Shape06[Ic64x];
        else
       if(IShape&0x01)Level=Shape05[Ic64x];
         else         Level=Shape04[Ic64x];
     else
        if(IShape&0x02)
       if(IShape&0x01)Level=Shape03[Ic64x];
         else         Level=Shape02[Ic64x];
        else
       if(IShape&0x01)Level=Shape01[Ic64x];
         else         Level=Shape00[Ic64x];
//---------------------------------------------------------------------
// Control Signals Gereration (Based on Desired Level)
  Mux1=0x00;
  Mux2=0x00;
  if(Level&0x01)Mux1=Mux1|0x01; else Mux1=Mux1|0x02;
  if(Level&0x02)Mux1=Mux1|0x04; else Mux1=Mux1|0x08;
  if(Level&0x04)Mux1=Mux1|0x10; else Mux1=Mux1|0x20;
```

```
  if(Level&0x08)Mux1=Mux1|0x40; else Mux1=Mux1|0x80;
  if(Level&0x10)Mux2=Mux2|0x40; else Mux2=Mux2|0x80;

//---------------------------------------------------------------------
//  Switching MUX
if(STOPC==0){       //  MUX Switching
     if(INT_MODOMUX==0){                  // All off
            PORTC = 0x00;
            PORTB&= 0x3F;
     }
     if(INT_MODOMUX==1){                              // Output = 0v (short-circuit)
      Mux1=0xAA ; Mux2=0x80;                          // Output = 0V (short-circuit)
            Iaux  = (Mux2&Mux2a)|0x3F;
            PORTC  = (Mux1&Mux1a); PORTB&=Iaux;
            asm("nop");asm("nop");asm("nop");asm("nop");
            asm("nop");asm("nop");asm("nop");
            PORTC  = Mux1;        PORTB|=Mux2;
            Mux1a = Mux1;
            Mux2a = Mux2;
     }
     if(INT_MODOMUX==2){                             // Normal Operation
            if(Ic64x>(IPdelay+1)){     // normal (until time one step before delay)
             Iaux  = (Mux2&Mux2a)|0x3F;
             PORTC  = (Mux1&Mux1a); PORTB&=Iaux;
             asm("nop");asm("nop");asm("nop");asm("nop");
             asm("nop");asm("nop");asm("nop");
             PORTC  = Mux1;        PORTB|=Mux2;
             Mux1a = Mux1;
             Mux2a = Mux2;
     }
     else{
       Mux1=0xAA ; Mux2=0x80;                         // Output = 0V  (short-circuit)
            Iaux  = (Mux2&Mux2a)|0x3F;
            PORTC  = (Mux1&Mux1a); PORTB&=Iaux;
            asm("nop");asm("nop");asm("nop");asm("nop");
            asm("nop");asm("nop");asm("nop");
            PORTC  = Mux1;        PORTB|=Mux2;
            Mux1a = Mux1;
            Mux2a = Mux2;
      }
  } // Closes else if(Ic64x
}  // Closes if(STOPC==0)
//---------------------------------------------------------------------
//  Counters Processing
  Ic64++;
  Ic256++;
  if(Ic64>63){
    Ic64=0;
      Ic3++;
      if(Ic3==3){  // Begin of last quarter (negativ maximum)
      Vmed=IVmed; Imed=IImed;
      IVmed=0; IImed=0;
        Tctr=1;   // Enable Control Routine
        if(STOPC)STOPC--; // each 1/50
     }       // closes IC3==3
     if(Ic3>3){
       Ic3=0;
       Ic256=0;
     }
  }      // closes IC4 > 63
  if(Ic3&0x01)Ic64x = 63 - Ic64;
  else        Ic64x = Ic64;
//---------------------------------------------------------------------
// INT.TIMER2: Waveform Parameters update
  if(Ic3==0)if(Ic64==0){
    IPdelay                         = Pdelay;
      IShape                        = Shape;
      INT_MODOMUX    = CMUX;
  }
//---------------------------------------------------------------------
// INT.TIMER2: UCaux treatment
 if(STOPC<150)clearbit(PORTA,6);                  // Ucaux Feedback


//---------------------------------------------------------------------
// Read A/D Converter and Measurements
```

```
 if(Ic256==125){
   ADMUX = 0x01;               //Select channel: Battery voltage
   Ad_Vbat=3;while(Ad_Vbat--);  // Sample Time
   ADCSR |= 0x40;              //Start conversion
   while(!(ADCSR & BIT(ADIF))); //Check if converstion is ready
   Ad_Vbat=ADCL;               //Read 8 low bits first (important)
   Ad_Vbat|=(int)ADCH << 8;     //Read 2 high bits and shift into top byte
 }
// else
// if(Ic256==129){
//   ADMUX = 0x04;               //Select channel: Temperature
//   Ad_Temp=3;while(Ad_Temp--);  // Sample Time
//   ADCSR |= 0x40;              //Start conversion
//   while(!(ADCSR & BIT(ADIF))); //Check if converstion is ready
//   Ad_Temp=ADCL;               //Read 8 low bits first (important)
//   Ad_Temp|=(int)ADCH << 8;     //Read 2 high bits and shift into top byte
// }
 else
 if(Ic256&0x01){                                          // Read Voltage at ODD instants
   ADMUX = 0x02;               //Select channel: Output voltage
   Ad_Vout=3;while(Ad_Vout--);  // Sample Time
   ADCSR |= 0x40;              //Start conversion
   while(!(ADCSR & BIT(ADIF))); //Check if converstion is ready
   Ad_Vout=(ADCL>>1);          //Read 8 low bits first (important)
   Ad_Vout|=(int)ADCH << 7;     //Read 2 high bits and shift into top byte
   IVmed = IVmed + Ad_Vout;     // Mean (1 cycle)
   II16+=II;                                                 // Current Measurement: 0 to 511
   Ic16++;
   if(Ic16>15){
              Ic16=0;II16=0;
   }
 }
 else{                                                       // Read Current at EVEN instants
  ADMUX = 0x00;               // Select channel: Input Current
  Ad_Ibat=3;while(Ad_Ibat--);  // Sample Time
  ADCSR |= 0x40;              //Start conversion
  while(!(ADCSR & BIT(ADIF))); //Check if convertion is ready
  Ad_Ibat=(ADCL>>1);          //Read 8 low bits first (important)
  Ad_Ibat|=(int)ADCH << 7;     //Read 2 high bits and shift into top byte
  if(Ad_Ibat>=Ioffset){II=Ad_Ibat-Ioffset;}
  else                                    {II=Ioffset-Ad_Ibat;}
  IImed=IImed+II;                          // Mean of Module(1 cycle)
 }
//---------------------------------------------------------------------
//  Protections
 if(II16>LI16)ERROR|=0x04;  // Current Protection (1.2ms Average)
 if(ERROR)if(STOPC<3){
    ONOFF=0;                  // Not really necessary(will be done next),but...
      STOPC=200;              // Not really necessary(will be done next),but...
    setbit(PORTD,3); // Turn Drives OFF (only Full-bridge)
    PORTD&=0x0F;     // Turn off all Full-Bridge MOS
 }
//---------------------------------------------------------------------
} // close void timer2_comp_isr(void)
```

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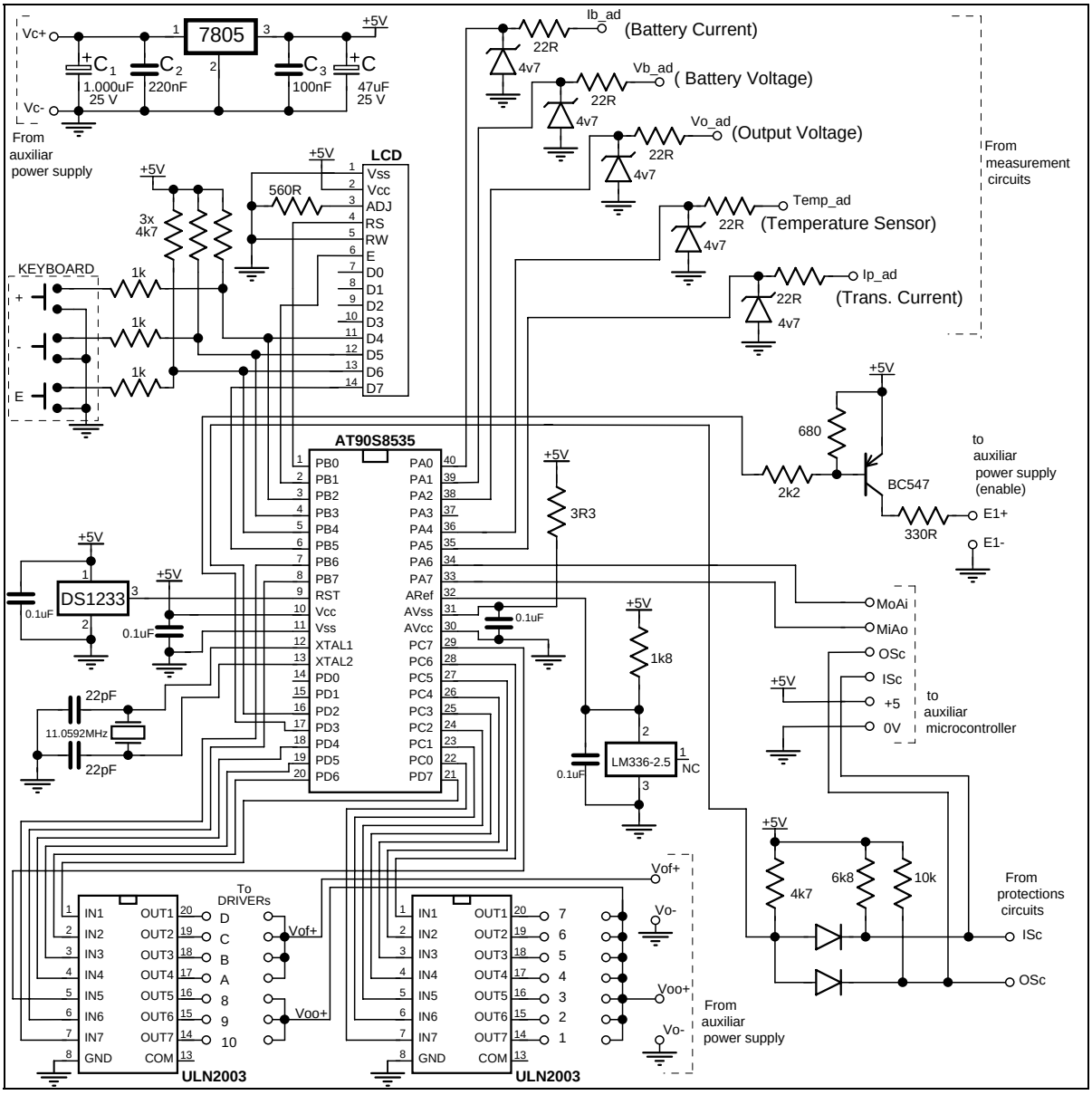
Appendix E
Pseudo-code for signals generation (p = 27)

```
% Pseudo-code for p = 27

I sa=H sb=L sc=H sd=L
I  1=L 2=H 3=L 4=H;
I  5=L 6=H 7=L 8=H;
I  9=L 10=H;

S 20e-3   2000e-9   100e-9   12.0;

T 0.000350000   sc=b  sd=e;

T    0.00035          2=e 1=a;
T    0.000355         1=e 2=a  4=e 3=a;
T    0.00036          2=e 1=a;
T    0.000422628      1=e 2=a  3=e 4=a   6=e 5=a;
T    0.000541503      2=e 1=a;
T    0.000661132      1=e 2=a  4=e 3=a;
T    0.000781702      2=e 1=a;
T    0.000903412      1=e 2=a  3=e 4=a  5=e 6=a  8=e 7=a;
T    0.00102648       2=e 1=a;
T    0.001151143      1=e 2=a  4=e 3=a;
T    0.001277663      2=e 1=a;
T    0.001406338      1=e 2=a  3=e 4=a   6=e 5=a;
T    0.001537502      2=e 1=a;
T    0.001671543      1=e 2=a  4=e 3=a;
T    0.001808916      2=e 1=a;
T    0.001950158      1=e 2=a  3=e 4=a  5=e 6=a  7=e 8=a  10=e 9=a;
T    0.002095923      2=e 1=a;
T    0.002247014      1=e 2=a  4=e 3=a;
T    0.002404446      2=e 1=a;
T    0.002569536      1=e 2=a  3=e 4=a   6=e 5=a;
T    0.002744047      2=e 1=a;
T    0.002930445      1=e 2=a  4=e 3=a;
T    0.003132363      2=e 1=a;
T    0.003355581      1=e 2=a  3=e 4=a  5=e 6=a 8=e 7=a;
T    0.00361037       2=e 1=a;
T    0.003918768      1=e 2=a  4=e 3=a;
T    0.004425465      2=e 1=a;
T    0.005574535      1=e 2=a;
T    0.006081232      2=e 1=a  3=e 4=a;
T    0.00638963       1=e 2=a;
T    0.006644419      2=e 1=a  4=e 3=a  6=e 5=a  7=e 8=a;
T    0.006867637      1=e 2=a;
T    0.007069555      2=e 1=a  3=e 4=a;
T    0.007255953      1=e 2=a;
T    0.007430464      2=e 1=a  4=e 3=a  5=e  6=a;
T    0.007595554      1=e 2=a;
T    0.007752986      2=e 1=a  3=e 4=a;
T    0.007904077      1=e 2=a;
T    0.008049842      2=e 1=a  4=e 3=a  6=e 5=a  8=e 7=a  9=e 10=a;
T    0.008191084      1=e 2=a;
T    0.008328457      2=e 1=a  3=e 4=a;
T    0.008462498      1=e 2=a;
T    0.008593662      2=e 1=a  4=e 3=a  5=e  6=a;
T    0.008722337      1=e 2=a;
T    0.008848857      2=e 1=a  3=e 4=a;
T    0.00897352       1=e 2=a;
T    0.009096588      2=e 1=a  4=e 3=a  6=e 5=a 7=e 8=a;
T    0.009218298      1=e 2=a;
T    0.009338868      2=e 1=a  3=e 4=a;
T    0.009458497      1=e 2=a;
T    0.009577372      2=e 1=a  4=e 3=a  5=e  6=a;
T    0.00964          1=e 2=a;
T    0.009645         2=e 1=a  3=e 4=a;
T    0.00965          1=e 2=a;

T 0.009650000   sa=b  sb=e;
T 0.010350000   sd=b  sc=e;

T    0.01035          2=e 1=a;
T    0.010355         1=e 2=a  4=e 3=a;
T    0.01036          2=e 1=a;
```

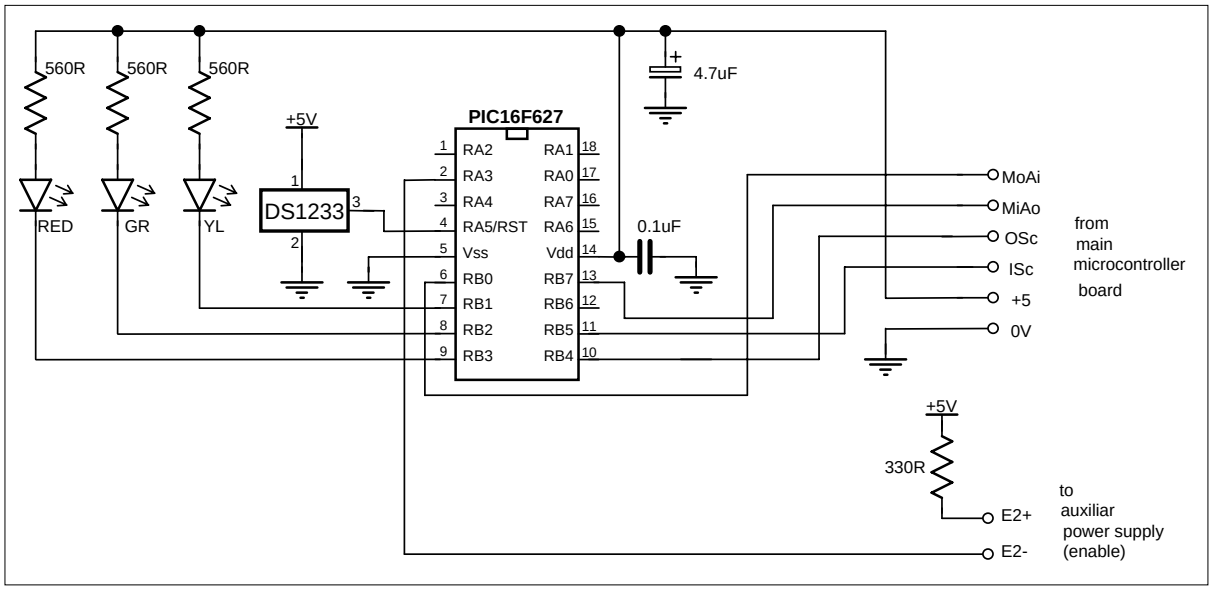
```
T   0.010422628     1=e 2=a  3=e 4=a   6=e 5=a;
T   0.010541503     2=e 1=a;
T   0.010661132     1=e 2=a  4=e 3=a;
T   0.010781702     2=e 1=a;
T   0.010903412     1=e 2=a  3=e 4=a  5=e 6=a  8=e 7=a;
T   0.01102648      2=e 1=a;
T   0.011151143     1=e 2=a  4=e 3=a;
T   0.011277663     2=e 1=a;
T   0.011406338     1=e 2=a  3=e 4=a   6=e 5=a;
T   0.011537502     2=e 1=a;
T   0.011671543     1=e 2=a  4=e 3=a;
T   0.011808916     2=e 1=a;
T   0.011950158     1=e 2=a  3=e 4=a  5=e 6=a  7=e 8=a  10=e 9=a;
T   0.012095923     2=e 1=a;
T   0.012247014     1=e 2=a  4=e 3=a;
T   0.012404446     2=e 1=a;
T   0.012569536     1=e 2=a  3=e 4=a   6=e 5=a;
T   0.012744047     2=e 1=a;
T   0.012930445     1=e 2=a  4=e 3=a;
T   0.013132363     2=e 1=a;
T   0.013355581     1=e 2=a  3=e 4=a  5=e 6=a 8=e 7=a;
T   0.01361037      2=e 1=a;
T   0.013918768     1=e 2=a  4=e 3=a;
T   0.014425465     2=e 1=a;
T   0.015574535     1=e 2=a;
T   0.016081232     2=e 1=a  3=e 4=a;
T   0.01638963      1=e 2=a;
T   0.016644419     2=e 1=a  4=e 3=a  6=e 5=a  7=e 8=a;
T   0.016867637     1=e 2=a;
T   0.017069555     2=e 1=a  3=e 4=a;
T   0.017255953     1=e 2=a;
T   0.017430464     2=e 1=a  4=e 3=a  5=e  6=a;
T   0.017595554     1=e 2=a;
T   0.017752986     2=e 1=a  3=e 4=a;
T   0.017904077     1=e 2=a;
T   0.018049842     2=e 1=a  4=e 3=a  6=e 5=a  8=e 7=a  9=e 10=a;
T   0.018191084     1=e 2=a;
T   0.018328457     2=e 1=a  3=e 4=a;
T   0.018462498     1=e 2=a;
T   0.018593662     2=e 1=a  4=e 3=a  5=e  6=a;
T   0.018722337     1=e 2=a;
T   0.018848857     2=e 1=a  3=e 4=a;
T   0.01897352      1=e 2=a;
T   0.019096588     2=e 1=a  4=e 3=a  6=e 5=a 7=e 8=a;
T   0.019218298     1=e 2=a;
T   0.019338868     2=e 1=a  3=e 4=a;
T   0.019458497     1=e 2=a;
T   0.019577372     2=e 1=a  4=e 3=a  5=e  6=a;
T   0.01964         1=e 2=a;
T   0.019645        2=e 1=a  3=e 4=a;
T   0.01965         1=e 2=a;


T 0.019650000   sb=b  sa=e;
```

Appendix F
Schematic circuits

Schematic of main controller

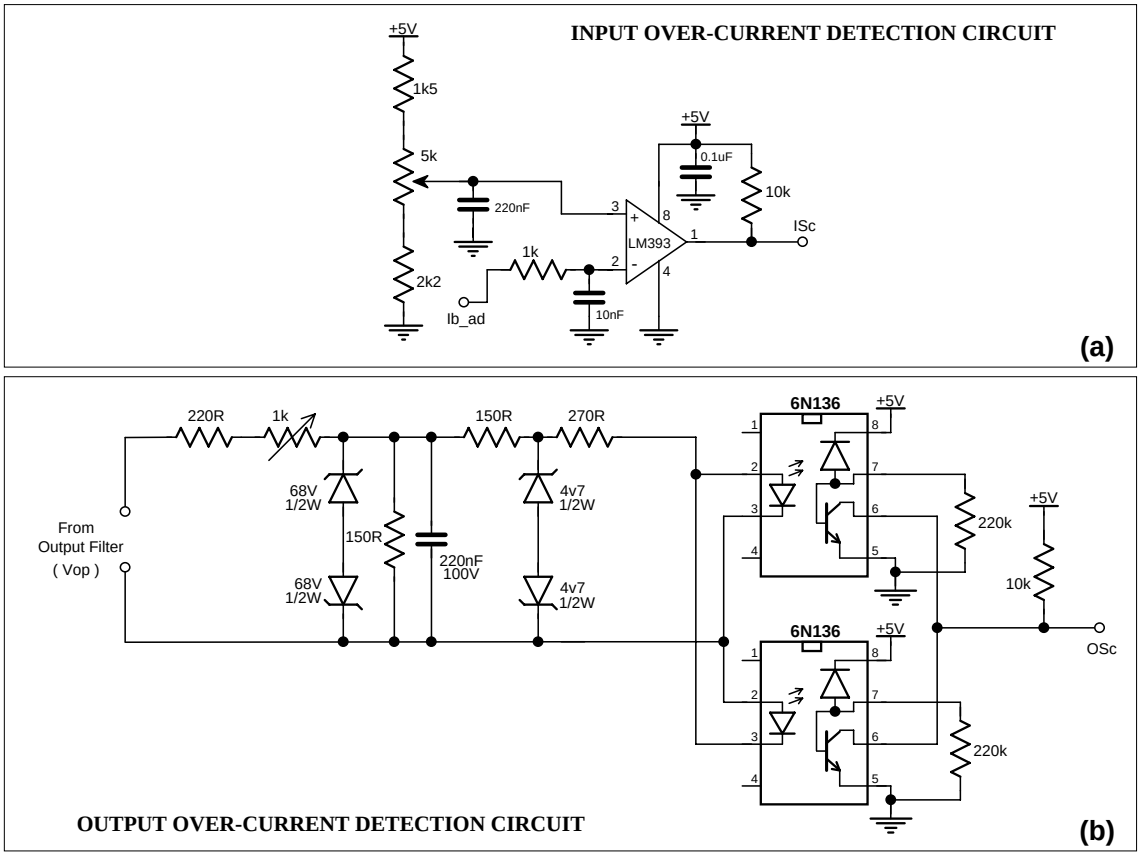


Schematic of auxiliary controller



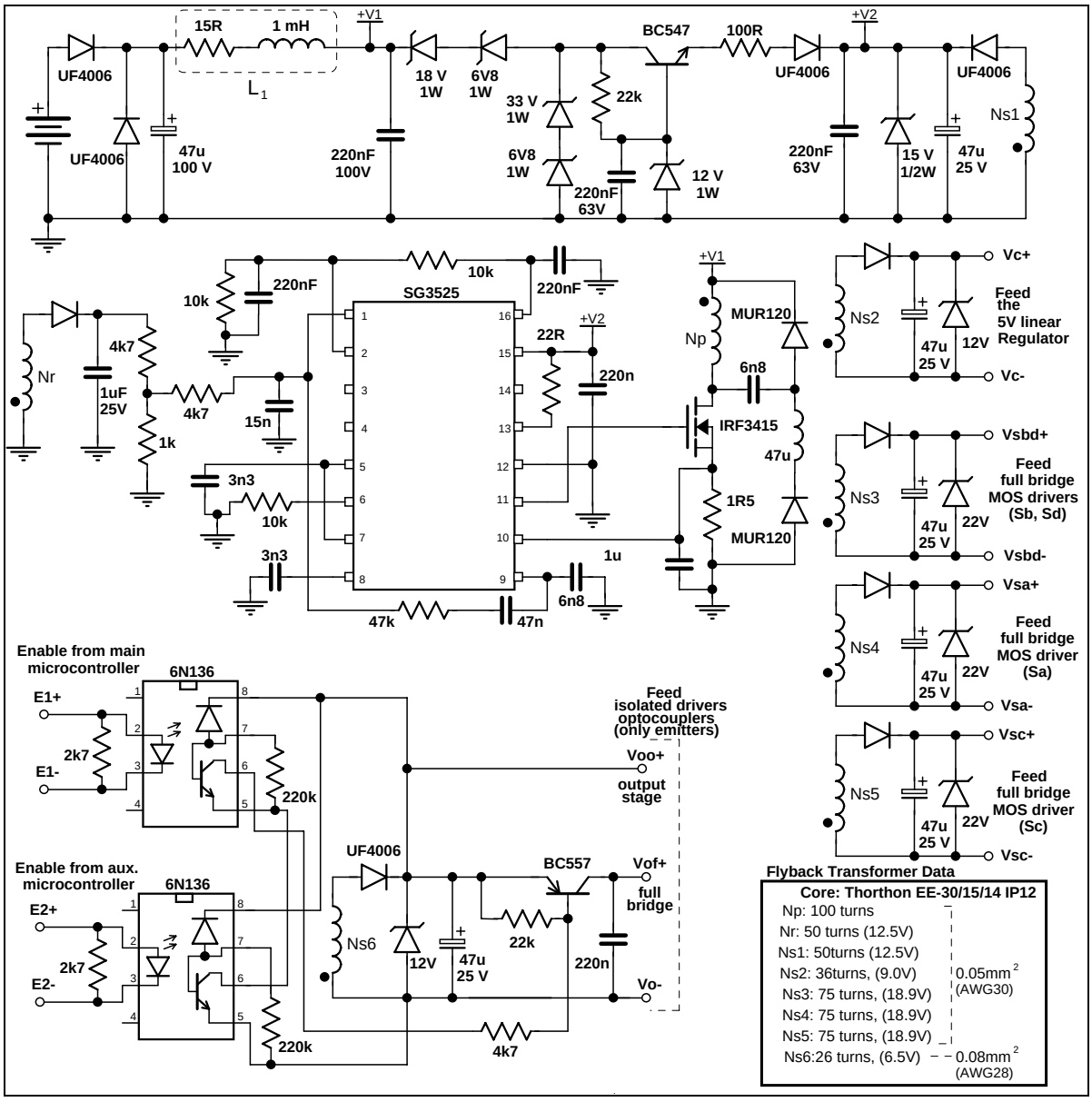
Over-current protection circuits

The implemented prototype is protected against over-current conditions at its input and output by using the circuits shown in figures (a) and (b), respectively. The input protection circuit makes use of the battery current sensor. It simply compares the sensor output with an adjustable voltage reference and generates a pulse that is applied to both main and auxiliary microcontrollers. It should be noted that this circuit only detects an over-current in one direction (in this case, from the battery to the converter).



The output protection circuit is connected in parallel with the output filter inductor and it is less accurate then the input protection circuit. In fact, it will act only if a fast and large change in the load occurs, such as the case of short-circuit. In this case, the voltage developed across the output filter inductor will be enough to turn on one of the optocouplers, thus generating a quick output pulse.

Auxiliary power supply schematic (flyback converter)



Appendix G
Transformer optimization calculation sheet
(MATLAB 5.3.0.620a (R11) - Student Edition)

```
% Experimental data used (Efficiency x power)
% File: n48v.mat
%|---------------      Experimental        ----------|
%   Pout                        Efficiency[%]
%   60                          76.27
%   120                         86.36
%   238                         92.3
%   297                         93.52
%   355                         94.31
%   449                         95.08
%   561                         95.59
%   673                         95.84
%   783                         95.95
%   945                         96
%   1057                        95.93
%   1167                        96.01
%   1275                        95.86
%   1359                        95.72
%   1463                        95.53
%   1565                        95.33
%   1666                        95.12
%   1917                        94.7
%   2015                        94.48
%   2112                        94.24
%   2208                        94
%   2283                        94.01
%   2377                        93.76
%   2469                        93.49
%   2560                        93.23
%   2631                        93.02
%   2808                        92.51
%   2963                        92.07
%   3318                        91.24
%   3475                        90.73


% Experimental and estimated data used in this analisys
% No load consumption and so on.
% File: trafo.mat
%|----------- Experimental ----------|  |----------------------------------------- Estimated -----------|
%Vb         xxx             xxx             PNL[W]      R change Factor   Estimated R
%36         7.5             8.52              11.10       1.870277778     0.033665
%38         8.31            9.44              12.02       1.6726512       0.030107722
%40         9.1             10.33             12.92       1.501666667     0.02703
%42         10.06           11.43             14.01       1.352372449     0.024342704
%44         11.17           12.69             15.27       1.220915978     0.021976488
%44.64     11.59           13.16             15.75       1.182103029     0.021277855
%46         12.47           14.16             16.75       1.104263548     0.019876744
%48         14.1            16.02             18.60       1               0.018          %Base model: 18mOhm
%50         16.5            18.75             21.32       0.906183333     0.0163113
%52         20.3            23.06             25.65       0.821237673     0.014782278

clear all;

E = 1:5:1000;                   % Monthly consumption range
P = 1:1:3500;                   % Load power range

%-------------------------------------------------------------
%Happenecker Hof Data
A=[ 00 00 05 25 32 40 27 35 40 32   28 22 15  9  7  7  8  5  4  3   3  3  4  4  6  4  7  8  5  4   4  5  6  4  4  1  1  2  2  2    0  1  2  1  2  2
0  0  1  3      1  1  0  2  2  2  0  1  0  0     0  0  1  1  0  0  0  0  0  0 ];

  for i=1:1:70,
     for j=1:1:50,
        Ax(50*(i-1)+j)=A(i);
     end;
  end;
%-------------------------------------------------------------
load -ascii n48v.mat
NL = 18.6;
```

```
nc_schmid = 100*n48v(:,1)./(((n48v(:,1))./(0.01*n48v(:,2)))-NL);

polschmid=polyfit(n48v(:,1),nc_schmid,12);          %  EXPERIMENTAL DATA
FitSchmid = polyval(polschmid,n48v(:,1));
nmedschmid=0;
Area=0;
  for i=1:1:3500,
    fitncschmid(i) = polyval(polschmid,i);
    nmedschmid = nmedschmid + fitncschmid(i)*Ax(i);
    Area = Area + Ax(i);
  end;
nmedschmid = nmedschmid / Area
%figure(1); hold off;
%plot(n48v(:,1),n48v(:,2),'r');
%hold;


%plot(n48v(:,1),nc_schmid,'b');
%plot(10:1:3499,fitncschmid(10:3499),'g');
%grid;
%
%------------------------------------------------------------
load -ascii trafo.mat

polmag = polyfit(trafo(:,4),trafo(:,6),5);          % Estimated transformer Req[Ohm] x PNL[W]
Fitmag = polyval(polmag,10:1:20);                   % Fit Curve
figure(1); hold off;
plot(10:1:20,Fitmag,'g');
hold;
%plot(trafo(:,4),trafo(:,6),'*r');
%axis([10 20 0.010 0.055]);
hold;
grid;

poltra = polyfit(trafo(:,1),trafo(:,4),5);          % Inverter Characteristic PNL[W] x Vin[V]
Fittra = polyval(poltra,35:1:54);                   % Fit Curve
figure(2); hold off;
plot(35:1:54,Fittra,'g');
hold;
plot(trafo(:,1),trafo(:,4),'vr');
hold;
grid;

NL = 18.6;                                          % Nominal no-load
R = polyval(polmag,NL);                             % ReqxV characteristic
ntrafo186 = (P-R.*((P.^2)./(39.2^2)))./P;           % Rated Trafo Conversion Efficiency x power curve
figure(3); hold off;
plot(P,100*ntrafo186,'g');                          % Transformer conversion effic. x power curve (Model)
hold;
ninv186 = (P-(10.6)-R.*((P.^2)./(39.2^2)))./P;      % Transformer rated efficiency x power curve (Model)
plot(P(100:3500),100*ninv186(100:3500),'r');
plot(n48v(:,1),n48v(:,2),'b');                      % Inverter rated efficiency x power curve  (Experimental)



%NL = 12.0;
 for j=1:1:100,
  NL(j)=j/10+10; % 10W a 20W
  R(j) = polyval(polmag,NL(j));
  ntrafox = (P-R(j).*((P.^2)./(39.2^2)))./P;
  nw(j)=0;
  Area=0;
    for i=1:1:3500,
      nw(j) = nw(j) + (fitncschmid(i)*ntrafox(i)/ntrafo186(i))*Ax(i);
      Area = Area + Ax(i);
    end;
    nw(j) = nw(j) / Area;
  end;

figure(4);
hold off;
plot(NL,nw,'r');
axis([10 20 97.4 98.5]);
hold;
%plot(NL(j),nw(j),'r');
grid;
```

```
%-------------------------------------------------------------
EE=200;
Pw = 0.72.*NL + ((1-nw/100)./(nw/100)).*EE; [x,y]=min(Pw); nl1=NL(y)
figure(5); hold off;
plot(NL,Pw,'r');
hold;
EE=350;
Pw = 0.72.*NL + ((1-nw/100)./(nw/100)).*EE; [x,y]=min(Pw); nl2=NL(y)
plot(NL,Pw,'b');
EE=500;
Pw = 0.72.*NL + ((1-nw/100)./(nw/100)).*EE; [x,y]=min(Pw); nl3=NL(y)
plot(NL,Pw,'g');
grid;
%-------------------------------------------------------------
figure(6); hold off;
plot(n48v(:,1),n48v(:,2),'r');
hold;
axis([0 3000 80 97]);
%plot(10:1:3499,fitncschmid(10:3499),'g');
grid;


R1 = polyval(polmag,nl1)
ntrafox = (P-R1*((P.^2)./(39.2^2)))./P;
ncw=0;
Area=0;
for i=1:1:3500,
  nct1(i) = (fitncschmid(i)*ntrafox(i)/ntrafo186(i));
  nt1(i)  = 100*(i/(nl1 + 100*i/nct1(i)));
  ncw = ncw + nct1(i)*Ax(i);
  Area = Area + Ax(i);
end;
nmed1 = ncw / Area

R2 = polyval(polmag,nl2)
ntrafox = (P-R2*((P.^2)./(39.2^2)))./P;
ncw=0;
Area=0;
for i=1:1:3500,
  nct2(i) = (fitncschmid(i)*ntrafox(i)/ntrafo186(i));
  nt2(i)  = 100*(i/(nl2 + 100*i/nct2(i)));
  ncw = ncw + nct2(i)*Ax(i);
  Area = Area + Ax(i);
end;
nmed2 = ncw / Area

R3 = polyval(polmag,nl3)
ntrafox = (P-R3*((P.^2)./(39.2^2)))./P;
ncw=0;
Area=0;
for i=1:1:3500,
  nct3(i) = (fitncschmid(i)*ntrafox(i)/ntrafo186(i));
  nt3(i)  = 100*(i/(nl3 + 100*i/nct3(i)));
  ncw = ncw + nct3(i)*Ax(i);
  Area = Area + Ax(i);
end;
nmed3 = ncw / Area


%plot(10:3499,nct1(10:3499),'k');
plot(50:3499,nt1(50:3499),'k');
%plot(10:3499,nct2(10:3499),'k');
plot(50:3499,nt2(50:3499),'k');
%plot(10:3499,nct3(10:3499),'k');
plot(50:3499,nt3(50:3499),'k');

%-------------------------------------------------------------
n1 = 0.984;                     NL1=18.6;
n2 = 0.969;                     NL2=16;
n3 = 0.963;                     NL3=10;
n4 = nmed1/100;   NL4=nl1;
n5 = nmed2/100;   NL5=nl2;
n6 = nmed3/100;   NL6=nl3;


P1 = 0.72*NL1 + ((1-n1)/n1).*E;
P2 = 0.72*NL2 + ((1-n2)/n2).*E;
```

```
P3 = 0.72*NL3 + ((1-n3)/n3).*E;
P4 = 0.72*NL4 + ((1-n4)/n4).*E;
P5 = 0.72*NL5 + ((1-n5)/n5).*E;
P6 = 0.72*NL6 + ((1-n6)/n6).*E;

figure(7); hold off;
plot(E,P1,'r');
axis([0 500 6 20]);
hold;
plot(E,P2,'b');
plot(E,P3,'g');
plot(E,P4,'k');
plot(E,P5,'k');
plot(E,P6,'k');
grid;
%----------------------  END ------------------------
```

Biography

Sérgio Daher was born in Fortaleza-Brazil on the 3rd of August 1971; son of Elias Daher and Josephina Sophia Lira Daher. Since young, he showed interest in sciences and latter he gave special attention to the electrical and electronic engineering areas, what remains until today. His main areas of interest are: Power Electronics, Renewable Energy Systems, Electronic Instrumentation and Control Systems.

He believes that is possible to make the world better: all together, starting now, within our life context, doing small daily contributions.

Academic Studies

1986 - 1990 **Technical in Electricity** (15th January 1990)
Federal Technical School of Ceará - ETFCe - Fortaleza - Brazil

1990 - 1995 **Graduation in Electrical/Electronic Engineer** (28th January 1995)
Universidade Federal da Paraíba - UFPb - Campina Grande - Brazil

1995 - 1997 **Msc. in Electrical Engineer** (12th September 1997)
Universidade Federal do Ceará - UFC - Fortaleza - Brazil
"*A Small Wind Generator Based on a Three-phase Induction Machine for Isolated Operation*"

2002 - 2006 **Dr. -Ing. in Electrical Engineer** (Defense day: 28th June 2006)
Universität Kassel - Kassel - Germany
"Analysis, Design and Implementation of a High Efficiency Multilevel Converter for Renewable Energy Systems"

Lecturer Experience

2000 - 2003 **Assistant Lecturer - Department of Electrical Engineering - 20 hours**
Universidade Federal do Ceará - UFC - Fortaleza - Brazil
Electrical Machines, Electrical Measurements, Micro controlled Systems.

2001 - 2004 **Assistant Lecturer - Department of Electronic Engineering - 12 hours**
Universidade de Fortaleza - UNIFOR - Fortaleza - Brazil
Analog Control Systems, Discrete Control Systems, Orientation of Works.

Professional Experience

1996 - 1998 **Founder/Director/Engineer**
Elementar Engenharia Ltda - Fortaleza - CE - Brazil
Head of diverse projects: Electronic Traffic Controller, Monitored Security Access Control, Microcontroller Development Boards and others.

1999 - 2005 **Founder/Director/Engineer**
Dahaco Engenharia e Rep. Ltda - Fortaleza - CE - Brazil
Head of diverse projects: Industrial Controller for Wheat Mill Factory, Outdoor Electronic Panel, Dedicated Data-Acquisition System, Wireless Automation Syst. for Restaurants, Advanced Traffic Controller, and others.

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Kassel, 08th August 2006